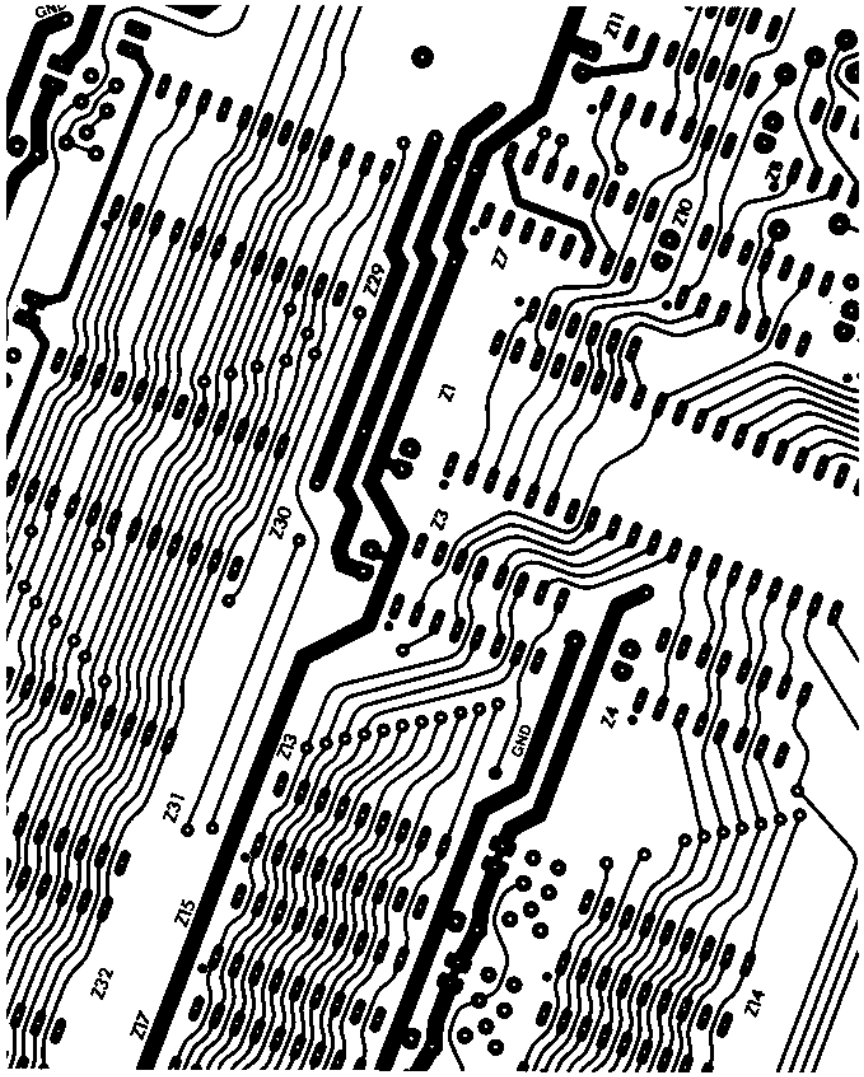
CHROMA™

Service Manual



CHROMA SERVICE MANUAL

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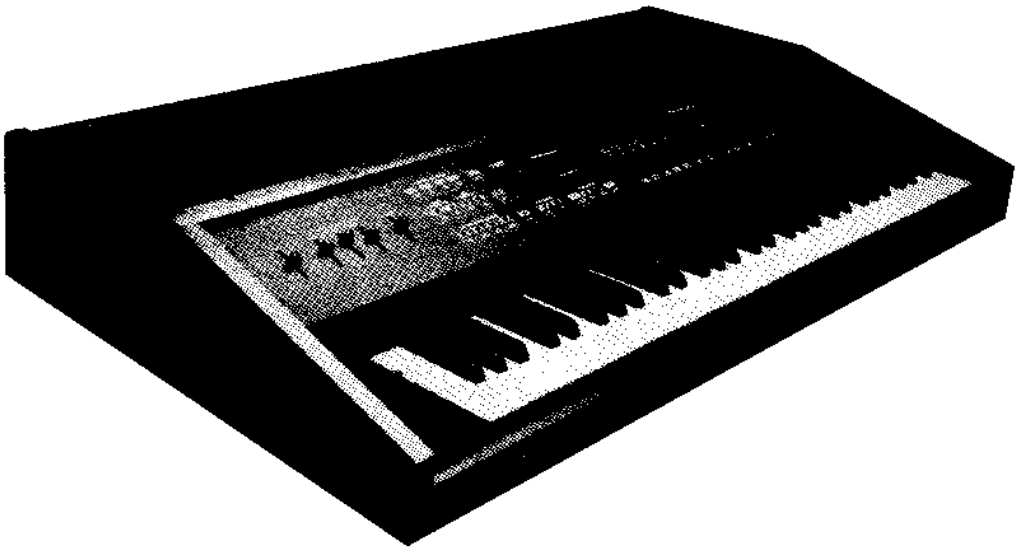


Chroma synthesizers are an extraordinary achievement of America's research and engineering sciences. The Chroma is a sixteen channel fully programmable polyphonic synthesizer with fifty preset sounds complete with touch responsive keyboard.

The Chroma is computer-based using two microprocessors, one for keyboard dynamics, the other for high-speed digital control of the analog channels.

In its most basic form, the Chroma consists of a computer (in the digital domain), synthesizer channels (in the analog domain) and input/output support hardware (interfacing between the digital and analog domains) as illustrated in Figure 1 - 1.

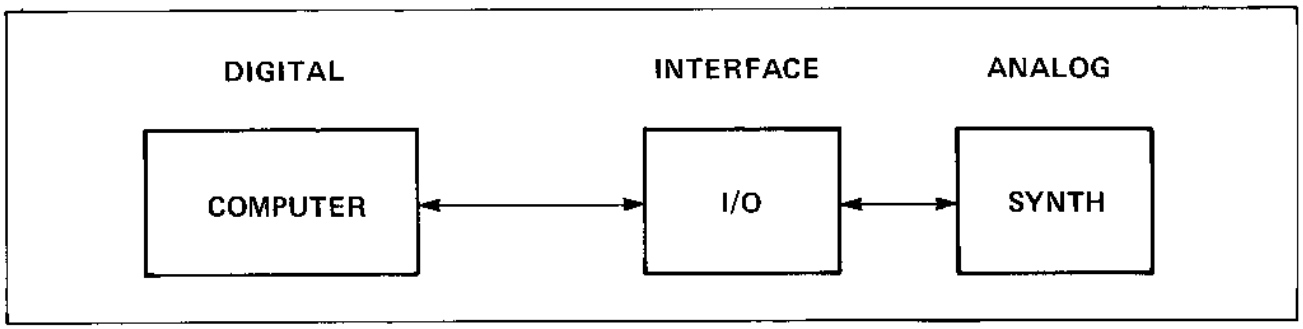


FIG. 1 - 1 BASIC SYSTEM

The computer consists of a central processing unit (CPU) and memory. The CPU is a 68B09 microprocessor clocked at 8MHz. Memory consists of 7K random access memory and 16K read only memory. RAM is divided into 4K NMOS for data structuring (read/write memory) and 3K CMOS non-volatile for storage of the fifty sounds. The 16K ROM contains the control program for the system using eight 2K EPROMs. The system is memory mapped and as shown in Figure 1 - 2 even the I/O read/write operations appear as memory locations to the 68B09.

Eight Dual Channel Boards make up the sixteen synthesizer channels. Each board contains two voltage controlled oscillators, two voltage controlled filters, two voltage controlled amplifiers, selectable waveforms and CMOS switching for versatile patching between circuits. These are supplemented with four envelope generators, two sweep generators (each capable of sixteen sweep waveforms from sine wave to random) and two glides per board. The envelopes, sweeps and glides are software generated, no hardware circuits exist for these functions. Figure 1 - 3 illustrates the basic architechture of a Dual Channel Board.

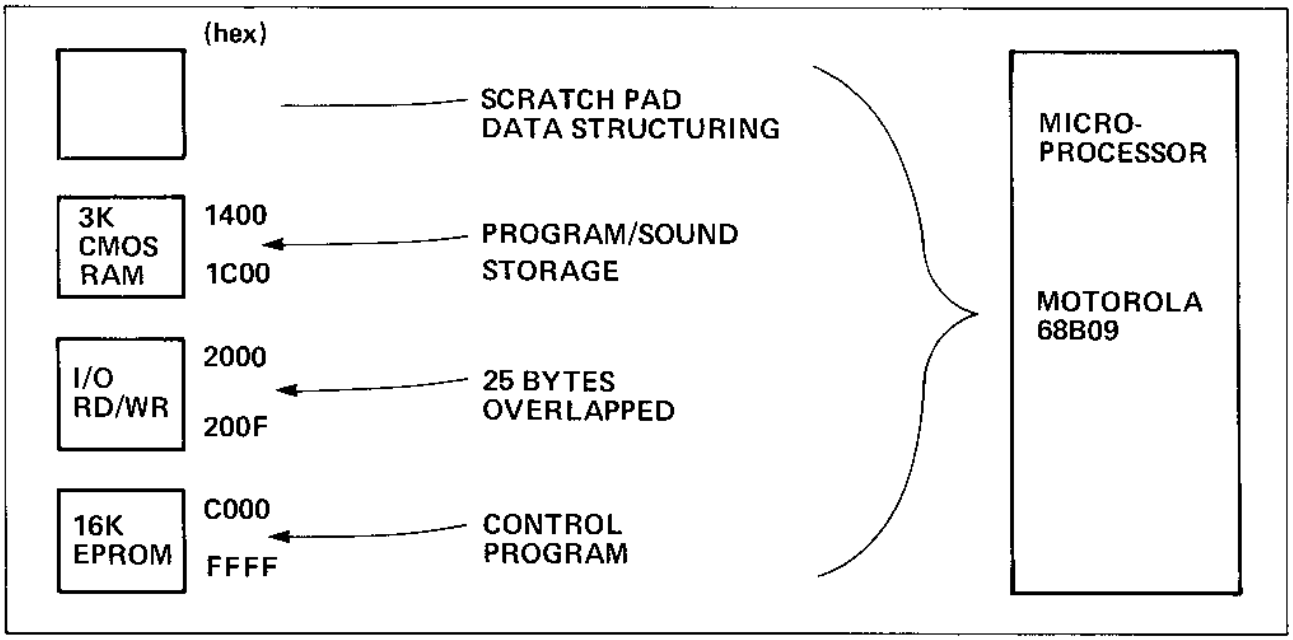


FIG. 1 - 2 CHROMA MEMORY MAPPED SYSTEM

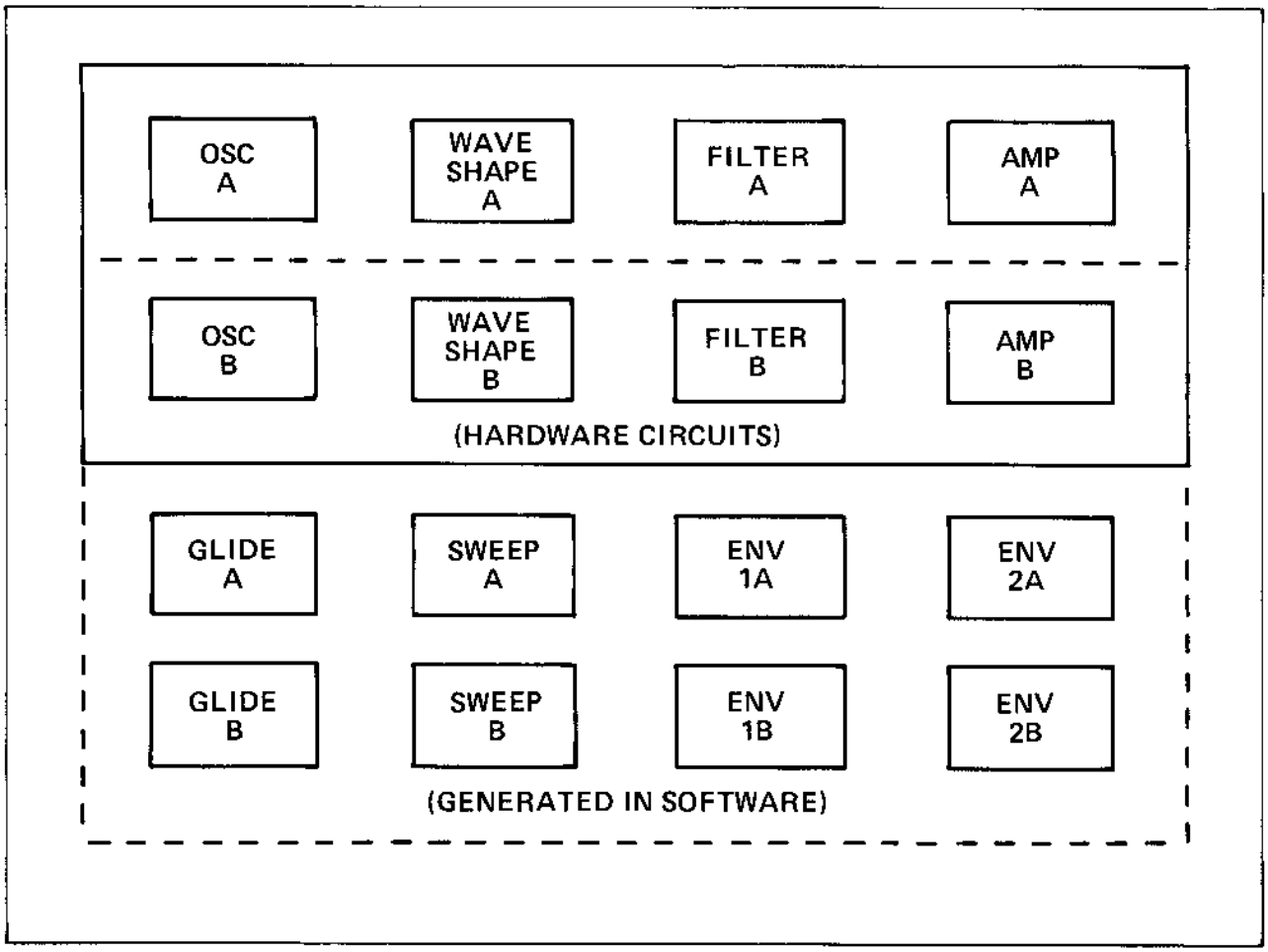


FIG. 1 - 3 DUAL CHANNEL BOARD BASIC ARCHITECTURE

The interconnections between the blocks shown in Figure 1 - 3 are a function of the preset sound selected or the sound programmed by the user. For example: Sweep "B" might go to Oscillator "A," Oscillator "A" to Filter "A," Filter "A" to Filter "B," Filter "B" to Amplifier "A," while Envelope "1B" might go to Filter "A" with Envelope "2A" going to Filter "B," etc. I think you get the idea. The patching is extremely versatile, the synthesizer very powerful. Remember, eight Dual Channel Boards result in thirty-two envelopes, and sixteen sweeps, oscillators, filters and amplifiers. The channel boards are divided into two sections, "A" and "B." The "A" section is controlled by "A" parameters and the "B" section by "B" parameters called up from the front panel individually or together.

The I/O or input/output chiefly consists of a keyboard scanning computer, a timer for cassette and auto-tune measurements and system timing, various decoders/drivers and two important converter circuits. The ADC or "A" to "D" converter looks at analog levels such as a slider or volume pedal and converts it to digital computer data. The DACs or "D" to "A" converters change digital computer data to analog voltages to operate the VCOs, VCFs and VCAs on the Dual Channel Boards. Figure 1 - 4 illustrates this handshaking.

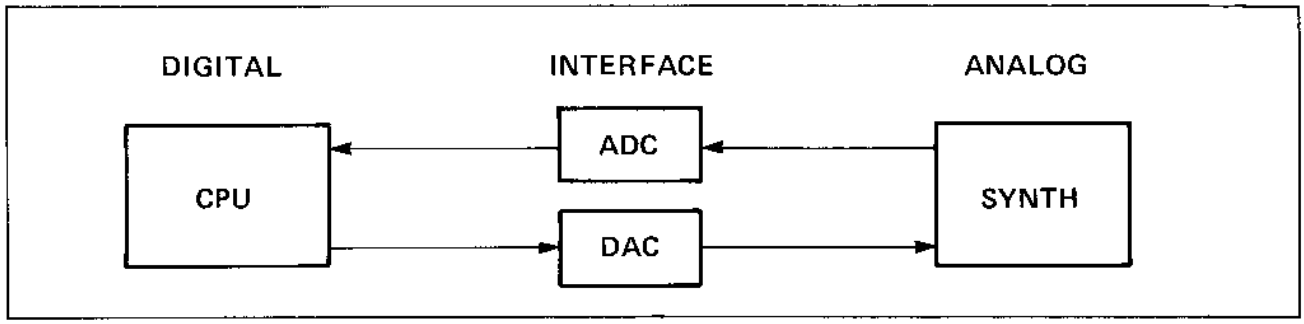


FIG. 1 - 4 SYSTEM INTERFACING

A system block diagram is shown in Figure 1 - 5. When a keyboard switch is depressed the keyboard scanning cmputer (Intel 8039) generates the note number and velocity then interrupts the CPU (Motorola 68B09). The CPU responds by fetching a vector address from EPROM memory which puts it into a sub-routine to read the note number then the velocity from the 8-bit bi-directional bus. The CPU manipulates this data using NMOS RAM under control of the EPROM firmware and writes digital data to the DACs for conversion to analog voltages. A serial stream of 64 discrete varying voltages from the DAC circuitry is continually sampled to provide oscillator pitch, pulse width, filter cutoff and volume. Other data structured by the CPU (influenced by the program selected from CMOS RAM) is written to the strobe decoder to establish the correct patches or interconnections on the Dual Channel Boards.

Control changes such as volume pedal, levers or sliders are read from the ADC by the CPU, manipulated in NMOS RAM, and subsequently change the sound. Changes in program selected or editing from the panel switch array, will also alter the data in NMOS RAM. This will affect the sound and change the display. The audio out from the Dual Channel Board is folded back during auto-tune operations to a zero crossing detector. The period of the output square wave is timed and read by the CPU. Pitch corrections are then written to the DACs for proper volts per octave and offset by the CPU. During auto-tune the CPU measures each of the sixteen oscillators twice, six octaves apart to establish correct volts per octave then a third time to adjust any offset. The filters are patched into self-resonance and also tuned during autotune. The entire auto-tune cycle takes about five seconds and should be done one or two times within an hour by the user. The timer also provides the CPU with cassette times for differentiating between the 1200Hz and 600Hz tones used to represent data bit levels on tape. Additionally, the timer helps regulate the main software loop.

Not shown on the system block diagram are the cassette interface, the audio EQ chain or the external computer interface. The external computer interface is a parallel port extending the 8-bit bi-directional bus complete with 8-bit input and output buffering. An expander module (with 8 more dual channels) may be connected to this port or an external computer may be connected for sequencing, multi-tracking, etc., or both expander and computer may be connected at the same time.

You can see from the previous description that the computer (68B09) is central to everything else in the system. Figure 1 - 6 illustrates the structure of the overall system.

An in-depth description of all Chroma circuits is detailed in Section 2.

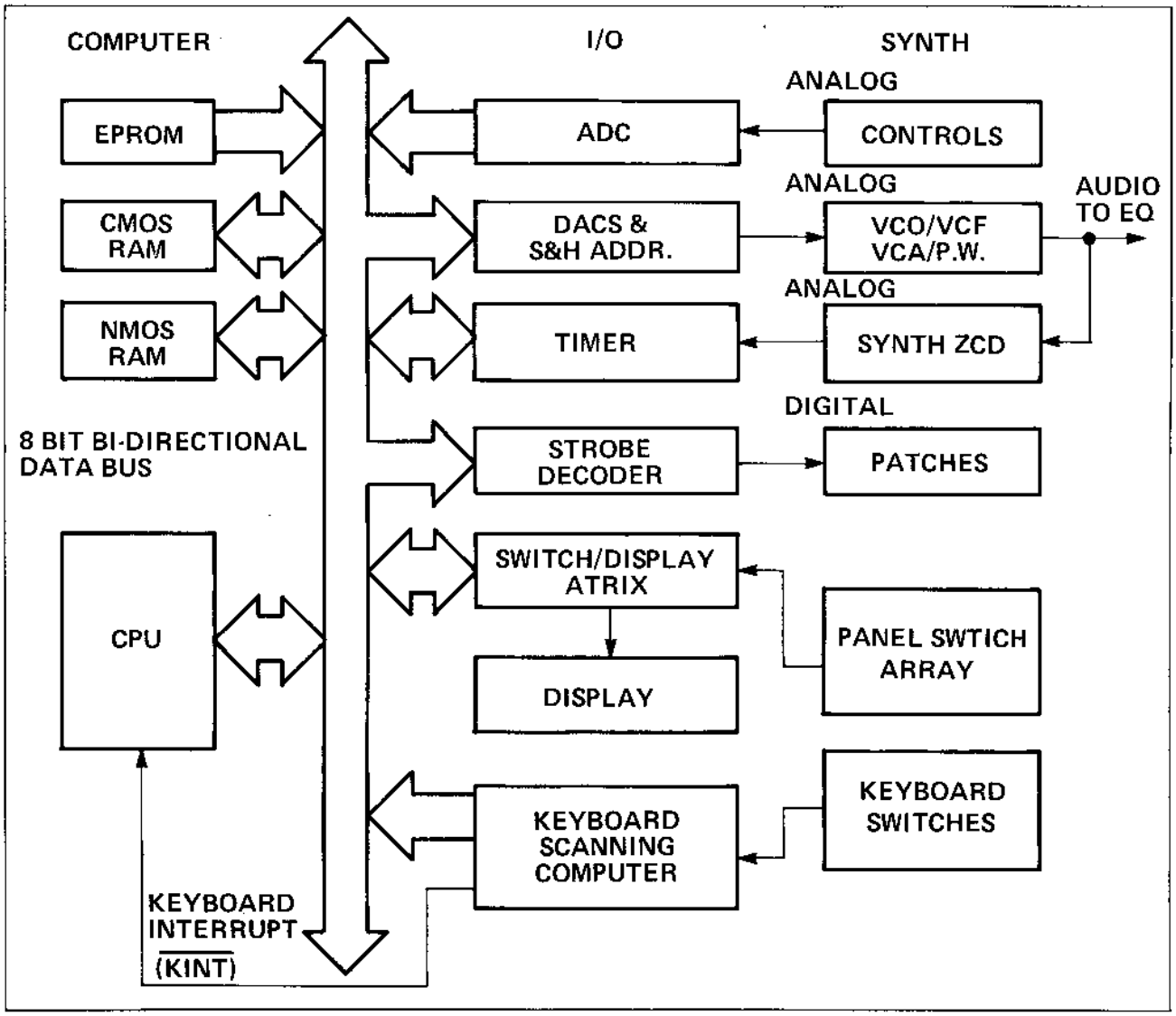


FIG. 1 - 5 SYSTEM BLOCK DIAGRAM

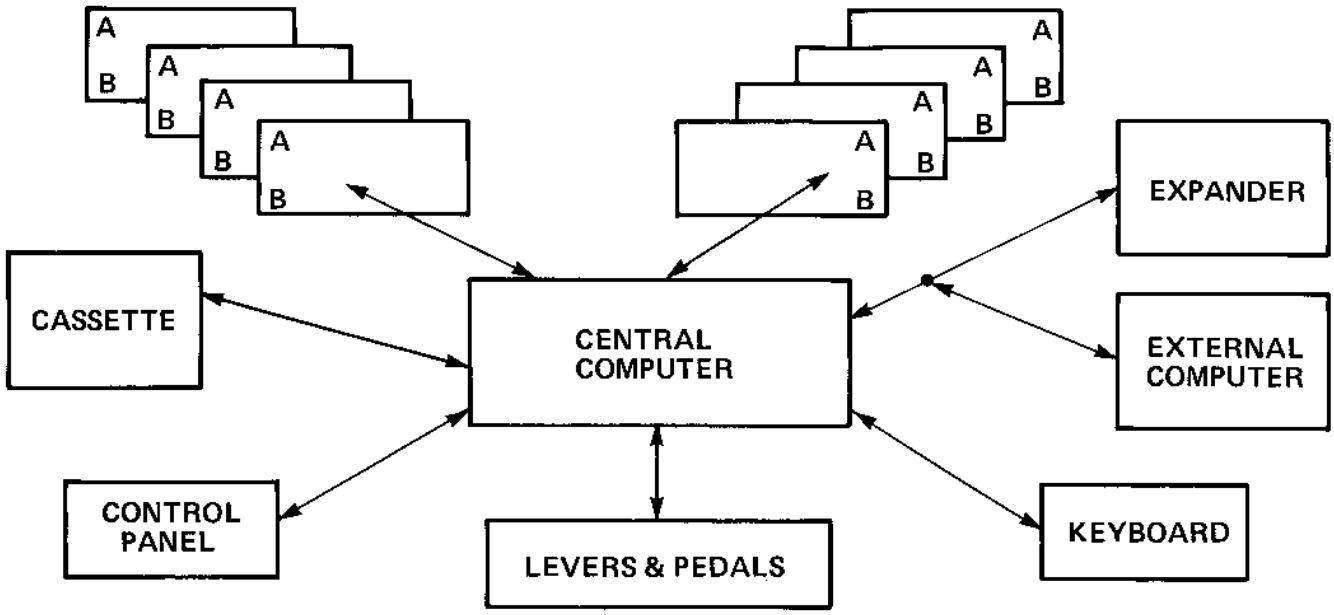


FIG. 1 - 6 SYSTEM STRUCTURE

COMPUTER BOARD

The Computer Board consists of the following sections, as outlined on the schematic:

1. Clock generator
2. CPU (central processing unit)
3. Address decoder
4. RAM
5. CMOS RAM
6. EPROM
7. CMOS RAM power switching

Each will be covered individually in the following descriptions.

1. CLOCK GENERATOR

The clock generator is a simple TTL crystal oscillator running at 16MHz. It feeds a divide-by-two flip-flop that produces a 2-phase 8MHz square wave, suitable for clocking both the 68B09 CPU on board and the 8039 keyboard scanning processor on the I/O board.

2. CENTRAL PROCESSING UNIT

The CPU circuit consists mainly of the 68B09 chip. Buffering is provided for the lower-order address lines, the control lines, and the data bus. The keyboard interrupt line ($\overline{KINT}$) drives the fast interrupt request ($\overline{FIRQ}$) line on the CPU. The external input and output interrupt lines ($\overline{XIINT}$ and $\overline{XOINT}$) both drive the normal interrupt request ($\overline{IRQ}$) pin on the CPU. The E and Q signals that emanate from the CPU consists of two 2MHz square waves in quadrature (90° out of phase), and these signals, "ORed" together by Z10A, provide a 75% duty cycle active-low enable signal that establishes the timing of each bus cycle. All on-board memories are connected to the CPU by the "direct bus" (D0 through D7). All off-board circuits are connected to the "buffered bus" (B0 through B7) which is isolated from the direct bus by a bus transceiver, Z2. This transceiver is enabled only when off-board devices are accessed. The circuit consisting of R44, R45, C31, Z8D and Z8F slightly delays the enable signal to the transceiver until the data output by the CPU chip is valid (during writes to off-board devices).

3. ADDRESS DECODER

The address decoder routes the 2MHz enable signal produced by Z10A to whatever device is being addressed during each bus cycle. The decoder is in two stages. The first stage consists of Z7, and routes the enable signal to one of it's eight outputs depending upon the three most significant address bits. Addresses in the range 0000 (hex) to 1FFF cause an enable pulse to be generated at pin 15, addresses in the range 2000 to 3FFF pulse pin 14, etc. The second stage consists of Z5 and Z6. Z5 is activated by addresses in the range C000 to FFFF and routes the signal to one of the eight EPROMs on the board. (The R/$\overline{W}$ signal on pin 6 prevents any spurious write cycles from attempting to write into the EPROMs.) Z6 is activated by addresses in the range 0000 to 1FFF and routes the signal to one of the eight pairs of RAM sockets on the board. Pin 14 of Z7 is gated with both polarities of the R/W signal to produce IORD and IOWR. These signals activate the input/output devices on the I/O board. Note that all input/output is memory mapped in 68B09 systems.

4. RAM

The system uses 4K bytes of RAM for storage of data structures during operation. Eight 1K by 4 static RAM chips are used.

5. CMOS RAM

The system requires 3K bytes of non-volatile storage for the synthesizer "programs." This is provided by six 1K by 4 static RAM chips. These chips have their own VDD line which remains powered when all else is shut off. Each transistor circuit functions as an isolator for the chip selects. When $\overline{RESET}$ is low (which it naturally is when the power is shut off) the transistors allow the chip select ($\overline{CS}$) inputs to the CMOS RAMs to rest high (inactive) even though the enable signals from the address decoder are all low.

6. EPROM

The firmware that controls the operation of the 68B09 processor amounts to almost 16K bytes. This is contained in eight 2K by 8 EPROMs. Their only peculiarity is that they are read-only devices. Hence the W/$\overline{R}$ line is used to disable them during write cycles.

7. CMOS RAM POWER SWITCHING

This circuit contains two AA cells, which provides power to the CMOS RAMs when the instrument is turned off, and two transistors to select between the battery and the main power supply. When the instrument is off, the battery is supplying a few volts. This is applied through the germanium diode CR1 to the CMOS RAMs. Since the rest of the circuit has no power, everything else is at 0 volts, meaning that Q1 and CR2 are reversed biased. As soon as the main power starts to rise above the battery voltage, CR2 becomes foward biased and CR1 becomes reversed biased. Now the CMOS RAMs are being powered from the main supply. However, the drop across CR2 can be nearly a volt under load. When the system $\overline{RESET}$ signal disappears (goes high), Q2 and Q1 turn on, shorting out CR2 and applying the full 5 volts to the CMOS RAMs. Capacitor C3 slows down this final transition to 5 volts. When the power shuts

down, the process is reversed, and the first thing that happens is the arrival of the system $\overline{\text{RESET}}$ signal. CR2 is a power diode because the CMOS RAMs consume significant current during operation. CR1 is a germanium diode for it's lower voltage drop. (Also, it leaks about 10uA when the main power is on, trickle charging the batteries.)

I/O BOARD

The I/O Board consists of the following sections, as outlined on the schematic:

1. I/O STROBE DECODER
2. KEYBOARD SCANNING COMPUTER
3. COMPUTER INTERFACE
4. TIMER
5. A/D CONVERTER
6. D/A CONVERTER
7. SWITCH/DISPLAY MATRIX
8. CASSETTE I/O
9. CASSETTE MOTOR SENSE/CONTROL
10. LED DRIVERS
11. TAPPER DRIVER
12. MISCELLANEOUS I/O

Each will be covered individually in the following descriptions, with particular attention paid to the keyboard scanning computer and the timer.

1. I/O STROBE DECODER (sheet 1)

The main computer selects each device it wants to communicate with by using the I/O strobe decoder and the data bus. Whenever the computer wants to read a byte (8 bits) of information from any device not located on the computer board, it activates the $\overline{\text{IORD}}$ line by bringing it low for 375ns (nanoseconds). During this time, the address bits A0, A1, A2 and A3 will contain a number that identifies the device that the computer wants to read data from. The decoder (Z39 for reads) generates a pulse on one of its eight outputs that looks just like the $\overline{\text{IORD}}$ pulse: active-low TTL level, 375ns wide. In other words, the decoder steers the master $\overline{\text{IORD}}$ pulse from the computer to one of eight devices. Each individual $\overline{\text{RD}}$ pulse causes the appropriate device connected to the data bus to turn on its output drivers. At the instant the $\overline{\text{IORD}}$ pulse is over, the computer samples the data on the bus.

The computer writes data to devices in a similar manner, although of course, the direction of the data flow is the opposite. The computer will activate the $\overline{\text{IOWR}}$ line for 375ns, and during this time the four address bits will contain a number identifying the device that the data is to go to. The decoder chips (Z40 and Z41 for writes) steer this pulse to one of 16 places. Meanwhile, the computer also drives the data bus with data. Each $\overline{\text{WR}}$ strobe line causes the appropriate device to sample the data bus and pick up the data.

All communication between the computer and the "outside world" is performed by time-sharing or multiplexing data over eight bus lines, and each byte of data takes 375ns to transfer. (There is an additional 125ns idle time between bus cycles, which means that the bus can transfer data at up to 2 million bytes per second.) In order to "see" what's going on in a computer system, it is necessary to examine the data bus during a specific time slot, not just all the time. If you look at a data bus line with an oscilloscope (without triggering off anything in particular) you will not see anything meaningful. Debugging such circuits require as an absolute minimum a dual trace oscilloscope with enough bandwidth to trigger off and see submicrosecond events. The technique is to use one trace to trigger off and view one of the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ strobes, and then use the other trace to examine each data bit in turn to see whether it is at a logic 0 or 1 at the trailing edge of the strobe.

The three decoder chips thus provide eight read strobe lines and sixteen write strobe lines. After the first small production run, it was decided that one more bit of input to the computer was required. Z55, a triple three-input open-collector NAND gate was added to sense the EOC (end-of-conversion) output from the A/D converter (description 5). Whenever the computer performs a read from location 2008 hex, address bit A3 will be high during the $\overline{\text{IORD}}$ pulse. This will cause data bus B7 to be pulled low if the conversion is not complete.

2. KEYBOARD SCANNING COMPUTER (sheet 1)

The keyboard scanning in the Chroma is performed by a separate processor, an Intel 8039. This processor has its own local data bus (DB lines, pins 12 through 19) which connects the 8039 to its program memory (EPROM Z33) and to the keyswitch boards. The operation of this data bus is similar to the operation of the main data bus, except that there is no separate address bus. Instead, there are four control signals associated with the bus that control the timing of all data transfers in and out of the 8039. All bus cycles begin with the 8039 asserting ALE (Address Latch Enable, an active high pulse). During the pulse period, the bus will contain an address. (Certain bits in port 2 are also used, but the keyboard scanning firmware only requires 8 address bits.) The address latch (Z32) is responsible for holding the address during the data transfer portion of the cycle. Shortly after ALE goes low, the data transfer commences, under control of one of three active-low strobe lines, $\overline{\text{PSEN}}$ (program store enable), $\overline{\text{RD}}$ and $\overline{\text{WR}}$.

This particular circuit uses $\overline{\text{PSEN}}$ to enable the EPROM containing the keyboard scanning firmware. It also uses the $\overline{\text{RD}}$ strobe to fetch data from the keyswitch boards, but it uses this strobe in an unconventional manner. The keyswitch boards accept a 4 bit code that selects one of 16 banks of keyswitches, and returns eight lines corresponding to the switches within the selected bank. The amount of time it

takes to return this data is too long for the entire communication to take place within one bus cycle so it is done in two. The firmware actually reads two banks of switches in a row, an A bank and a B bank for a particular group of eight keys. A total of three cycles are used. In the first cycle, the computer supplies the number of a bank on the address lines, strobes $\overline{RD}$, and ignores the data that it receives. This effectively writes the data to latch Z35 which drives the keyswitch boards. On the second cycle, it supplies the number of the second bank on the address lines, strobes $\overline{RD}$, and reads in the data from the previous bank. The number of the second bank is latched by Z35. On the third cycle it reads the data that returns from the second bank.

The keyboard scanning computer scans the keys about 1000 times per second. It measures, for each key, the time between the opening of one switch contact and the closing of the opposite contact in millisecond increments. Whenever a contact closes, the key number and the time measurement is sent to the main computer. The port pins (P1 and P2) on the 8039 are used for this purpose. Whenever information is to be transmitted to the main computer, the 8039 supplies the time measurement on port 2 bits 6-0 (pins 21-24, 35-37). Bit 7 (pin 38) will be high for a release and low for an attack. It then puts the key number (from 0 to 63) on port 1 (pins 27-34) and then sets pin 34 high. Thus pin 34 produces a short negative-going pulse whenever new information is present. The two NAND gates (Z49) form a set/reset flip-flop that performs interrupt handshaking between the two computers. Whenever information is sent by the 8039, the pulse from pin 34 sets the flip-flop to one state, bringing $\overline{KINT}$ low and interrupting the main computer. The main computer temporarily suspends what it is doing and reads first the key number, and then the time measurement by activating the $\overline{RD\ NOTE}$ and $\overline{RD\ VEL}$ strobes. The $\overline{RD\ VEL}$ strobe sets the flip-flop to the opposite state, clearing the interrupt.

Note that the interrupt line $\overline{KINT}$ also connects to the interrupt pin ($\overline{INT}$, pin 6) on the 8039. This *does not* interrupt the 8039. Instead, this pin is used by the keyboard scanning firmware to check to see if the previous data transfer is complete. The $\overline{K\ MASK}$ line serves a simple purpose during auto-tune and cassette operations. When low, it holds the flip-flop in its reset state (Z49-8 high). This causes any keys played on the keyboard to be ignored by fooling the 8039 into thinking that its interrupts are being immediately handled. Thus, any notes accidentally struck while the Chroma is in auto-tune, for instance, will not "pile up" and suddenly be heard when the auto-tune is complete.

The only other details of the keyboard scanning circuit are the clock lines. The 8039 gets its clock in two-phase form at 8MHz from the main computer, so both computers are actually synchronized. This synchrony isn't important to the operation, but does save the cost of another crystal oscillator. The port 2 lines emanating from the 8039 are not static lines, and as such, have to be latched (whereas the port 1 lines are perfectly static). The port 2 data is always valid during the rise of ALE, and so the ALE signal is used to clock the data into latch Z36. The ALE signal, which runs at about 500KHz, is also used as a clock signal for the A/D converter, as it is a convenient frequency.

3. COMPUTER INTERFACE (sheet 1)

The computer interface consists of an 8-bit input port with handshaking and an 8-bit output port with handshaking. If you are wondering what the port might connect to, imagine it connected to an exact duplicate of itself; that is, imagine each input port line (mnemonics starting with XI) connecting to the corresponding output port line (mnemonics starting with XO) at the other end of the interface. The interface only consists of the output latch (Z26), the input tri-state driver (Z27) and the five NAND gates. (Z48, 49). The rest of the circuit is just for noise rejection and isolation when the power is shut off. When the Chroma wants to transmit a byte of data, it checks the $\overline{XO\ FULL}$ line to see if the last byte it sent has been received yet. When it has, it writes the byte into the latch with the $\overline{WR\ EXTO}$ strobe. This causes the flip-flop consisting of gates Z48-A and Z48-B to be set, and pulls the $\overline{XO\ FULL}$ line low. This tells the computer that the output port is full (and not to send any more data yet) and tells the other end of the interface that there is fresh data to be had. When the other end reads the data, it will pulse the acknowledge line $\overline{XO\ ACK}$, which resets the flip-flop and resets $\overline{XO\ FULL}$ high (inactive) again. This tells the computer that it can send another byte of data. The input interface performs the other side of the same task. When data arrives from the other end via the XI lines, the $\overline{XI\ FULL}$ line will go low, telling the computer the fresh data has arrived. When it reads it, using the $\overline{RD\ EXTI}$ strobe, the acknowledge $\overline{XI\ ACK}$ will be pulsed, causing the flip-flop at the other end to be cleared, and causing $\overline{XI\ FULL}$ to go high (inactive) again.

The remaining gates are used to generate interrupts. Normally, the Chroma is ready to accept data from the interface, and the $\overline{XI\ MASK}$ line is high (inactive). This means that an incoming byte, which is accompanied by $\overline{XI\ FULL}$ going low, will cause $\overline{XI\ INT}$ to go low, interrupting the main computer. The only time the computer activates $\overline{XI\ MASK}$ to prevent input interrupts is during auto-tune and cassette operations, or if the device at the other end of the interface is sending data faster then the Chroma can process it. Normally, the Chroma has no data to transmit, and if it does, the interface is usually ready for it, as signified by a high (inactive) $\overline{XO\ FULL}$. If, however, the Chroma has data to send and the output port is still full from the previous data transfer, the Chroma will only wait a short amount of time before it decides it has better things to do than wait around. When this happens, the Chroma will stash the byte of data in a

FIFO (first in first out) queue in its memory and set XO MASK high (inactive), thus unmasking output port interrupts. The output port interrupt (XO INT) occurs whenever the device at the other end of the interface gets around to reading the data off the interface and sending back an XO ACK pulse. Then the Chroma will take time out from whatever it is doing to pull a byte from the end of the FIFO queue and output it. Only when the queue is empty does the main computer mask output interrupts again by setting XO MASK low (active).

4. TIMER (sheet 1)

The Chroma uses a timer implemented with TTL MSI (medium-scale integration) parts, as there are no LSI (large-scale integration) timer chips available that perform the specific functions needed. The timer consists mainly of a 16 bit resettable counter running at 2MHz (Z44 and Z45), a 16 bit latch (Z46 and Z47) and a status flip-flop (Z50C and Z51B). The rest of the circuit simply connects these basic elements to various signals. The timer has five operational modes that the Chroma uses under different circumstances. The timer mode is set, and the timer's operation is started, by writing the appropriate number to the timer mode latch (Z42). The modes, as reflected in a binary number that appears on pins 7, 14 and 2 of Z42, are as follows:

0. 1024us mode -- used to regulate the speed of the main software loop during normal operation.

1. Tape mode -- used to measure the period of the signal received from the cassette during LOAD ONE and LOAD ALL operations.

2. Synth mode -- used to measure the period of the synthesizer signal during auto-tune.

3. Synth/64 mode -- used to measure the accumulated period of 64 cycles of a high frequency during auto-tune.

4. 416us mode -- used to regulate the frequency of the cassette signals generated during SAVE ONE and SAVE ALL operations.

Each mode shares the same timing resources: a resettable counter, a latch, and a status flip-flop. What differs is how they are connected together.

0: 1024us MODE

This mode is used to regulate the speed that the Chroma repeats its calculations for each synthesizer channel. If the currently selected program contains little modulation, the amount of time the computer will take to compute each sample of the control signals may only be a few hundred microseconds. In a very complex program, the computing time is much longer, although it doesn't often get any longer than a millisecond. When the computer begins the calculations, it sets the timer mode to zero. The write pulse, WR TMOD, also resets the counter to zero through Z50A and sets the flip-flop not ready (TRDY high). The timer is designed so that the current count will be latched and the counter reset whenever a negative pulse comes out of either data selector (Z43A or Z43B). In mode 0, this occurs when the counter reaches a count of 2048 and Z45-5 goes low. The falling edge of this signal is differentiated by R58, R65 and C18 into a *very* narrow pulse (about 50ns) which is routed through data selector Z43B. When the computer has finished its calculations for a particular synthesizer channel, it polls TRDY until it goes active (low), signifying that the 1024us time has expired.

1: TAPE MODE

This mode is used during cassette load operations to measure the signal received from the cassette. The cassette uses a simple FM (frequency modulation) scheme operating at 1200 baud (bits per second). A 1 bit is represented by a full cycle of 1200 HZ and a 0 bit is represented by a half cycle of 600 HZ. Thus, a 1 bit is received as two 416us periods between zero-crossings and a 0 bit is received as a single 833us period between zero-crossings. The tape signal is presented to the timer as two signals, one being the inversion of the other. Each signal is connected to a differentiating network to generate a tiny negative-going pulse on the fall of the signal. Since the two signals are out of phase, a pulse is generated on one edge by one RC network and on the other edge by the other RC network. The data selectors route these pulses into the timer where they cause the current count to be latched and the counter to be reset. When the computer senses that the timer is thus ready (TRDY low), it reads the two-byte time value (RD TIME and RD TIME+1). The RD TIME strobe automatically sets the timer not ready again (via Z50 pin 10) even while the next time period is being measured.

The leftmost bit of the counter (Z45 pin 9) is fed through its own differentiating network back to the status flip-flop. This is in case the cassette (or auto-tune) isn't generating any signal. When the timer overflows its maximum count of 32767 (about 16ms), this line causes the status flip-flop to be set ready and 0 to be latched as the time value.

2: SYNTH MODE

This mode functions similarly to the tape mode, except that the entire period of the incoming signal (in this case, from a synthesizer oscillator or filter) is measured, instead of the time between successive zero-crossings. In other words, the timer need only be latched and reset on falling edges of the incoming signal. Therefore, only one phase of the signal is used. Data selector Z43A selects the differentiated falling edge of the signal. The auto-tune routine first selects this mode (which always sets

the timer not ready) and waits for it to become ready. Meanwhile, it refreshes all the sample-and-holds on the synthesizer channels. When the timer becomes ready, it reads in the two-byte value. If the value is 0, it assumes that the channel isn't functioning properly and that the timer overflowed. If the value is non-zero, the channel is probably making sounds but the reading still isn't valid, as it isn't referenced to anything. However, reading the time value sets the timer not ready again, so, without reseting the timer mode, the auto-tune waits a second time for the timer to become ready. When it's ready this time, the reading will accurately reflect the amount of elapsed time since the previous reading.

3: SYNTH/64 MODE

This mode is exactly like the previous mode, except that the signal whose period is being measured comes from a six stage binary counter (Z11). This counter functions as a prescaler for measuring high frequencies produced by the synthesizer channels during auto-tune.

4: 416us MODE

This mode functions exactly like the 1024us mode with one difference. Since the mode number is 100 in binary (as compared to 000 for the 1024us mode), the line from Z42 pin 7 to Z51 pin 13 is high in this mode. The four-input NAND gate (Z51A), when thus enabled, produces a negative-going signal when the count reaches a count of 832. This is routed through data selector Z43A to set the timer ready. During cassette saves, the computer waits for the timer to be ready, performs the necessary serial output, and then reads the timer (to set it not ready without resetting the counter). Thus, the serial output occurs at a 2400Hz rate. To output a 1 bit, the computer outputs 2 consecutive transitions. To output a 0 bit, the computer leaves out the first transition, generating a half cycle at half the frequency.

5. A/D CONVERTER (sheet 2)

The analog to digital converter is responsible for measuring the physical position of the two levers, two variable positions, and the TUNE and PARAMETER CONTROL sliders on the panel. It is also wired up to measure the voltage from the pressure sensor assembly or from the CMOS RAM battery. The circuit consists mainly of an ADC 0809 converter chip, which is a CMOS device that operates on a single 5V supply. It includes an on-board 8-input multiplexer for selecting one of eight analog voltages, an 8-bit D/A converter and successive approximation register. The computer selects a voltage to be measured by writing a number to the A/D converter ($\overline{\text{WR ADCO}}$ is the strobe). This activates the ALE input on the chip which causes the channel select number to be latched. The same strobe also activates the start conversion (SC) input to the chip. In order to allow the analog signal time to settle internally, the computer repeats the strobe 2.5us later, just to make sure. Then the computer goes off and performs other functions while the converter converts the voltage (which must be between 0 and 5 volts) to a number between 0 and 255. This takes about 150us. The computer eventually comes back to it and reads the converted value using the $\overline{\text{RD ADCI}}$ strobe.

The inputs to the A/D converter are all buffered by op-amps. The levers produce a voltage swing that's only about 0 to 2 volts, so the lever inputs are amplifed. The pedal inputs require a pullup resistor, as the pedals contain nothing more that a potentiometer to ground, but these levels need no amplification. However, all these signals need to be clamped so that they don't exceed 5V. The transistors on the op-amp outputs provide this function, as they are powered from 5 volts while the op-amps are powered from 12V. This scheme is used because the voltage would otherwise definitely exceed 5V. The TUNE and PARAMETER CONTROL slider inputs come from sliders that are "hung" between 0 and 5 volts, because they don't require accurate clamping. There are, however, diodes on the slider buffer op-amp outputs to protect the A/D against catastrophic op-amp failure. The pressure input is buffered off-board. The remaining input, which comes from the battery, is buffered with a FET-input op-amp for two reasons. First, the op-amp input must not drain the battery. Second, when the power is shut off, the input must not pull the battery voltage down. The P-channel JFETs used in the op-amp allow the input to exceed the positive rail of the device without conducting current.

Z55A inverts the EOC (end of conversion) signal generated by the A/D converter chip and delivers it to the other two sections of Z55, shown on sheet 1 immediately above the I/O Strobe Decoder. This IC was added following the initial pilot production run to provide a means for the computer to sense if an analog to digital conversion is successful. A particular quirk of the 0809 converter chip is that it occasionally doesn't work! Since this is pretty much a random occurrence, rarely happening for two conversions in a row, the computer handles it by simply ignoring the bad conversion. Since each analog input is measured fifty times a second, occasionally doing only forty-nine conversions doesn't cause any problems.

6. D/A CONVERTER (sheet 2)

The digital to analog converter generates all the voltages that are needed to control the analog circuits on the synthesizer channel boards. The main DAC (Z24) is a 12-bit DAC that uses a FET-input op-amp for an output buffer. Since one lsb (least significant bit) change corresponds to about 1.25mv, it is necessary that the op-amp offset voltage be well below this level. A null trimmer is provided, and can be adjusted by putting a DVM (with 100uv resolution) between the two test points and adjusting for zero.

With a -5 volt reference on pin 17, the range of the DAC would be 0 to +5 volts (it inverts). The reference voltage can, however, be "trimmed" under computer control by the use of the other DAC, Z20. This 8-bit DAC has a reference of +5 volts and hence produces an output of 0V to -5V. Op-amp Z21B and associated resistors reduce this range to approximately -4.4V to -5V. If the 8-bit DAC is centered, the reference to the 12-bit DAC will be about 4.7V. The oscillators and filters are scaled such that each step of the 12-bit DAC value corresponds to a 32nd of a semitone in pitch, which is a nice easy number for a computer to deal with. (Perfect semitone scales can be generated by counting with the five least significant bits set to zero.) However, no analog circuit is perfectly accurate. In conventional analog synthesizers, trimmer potentiometers are provided to adjust the scale factor of the pitch (so that an octave is really an octave). In the Chroma, this trimming is done by the computer by outputting the appropriate number to the 8-bit DAC. Of course, tuning offset can be corrected for by adding or subtracting a constant from the number sent to the 12-bit DAC.

There is nothing fancy about the DAC circuit. The 8-bit DAC uses two CMOS 4-bit latches for its data, which are written into by the computer with the $\overline{\text{WR RDAC}}$ strobe. CMOS latches are used because the 7523 DAC requires higher than TTL voltage levels. The 12-bit DAC occupies two bytes in the computer's address space. The four most significant bits are written into with the $\overline{\text{WR MDAC}}$ strobe. The remaining bits are written into with the $\overline{\text{WR MDAC+1}}$ strobe. TTL latches suffice with 7541 type DACs.

7. SWITCH/DISPLAY MATRIX (sheet 2)

The 71 switches and 80 display segments on the Chroma panel are arranged in matrices. The 10 "columns" of the matrix are driven by the outputs of Z13, a BCD-to-decimal decoder with high-current open-collector outputs. The computer can select a bank of switches and a display digit by writing a number into latch Z17 (using the $\overline{\text{WR SDS}}$ strobe). The computer can then turn on any segments in the selected digit by writing a pattern of bits to latch Z15 (using the $\overline{\text{WR SEGS}}$ strobe). The two large digits (I1) require the full drive capability of the decoder and latch, but the small digits (I2) require less current. (Note that the latch is S-series Shottky, not LS.) This is the purpose of the resistor network Z14. The computer multiplexes the display every 20ms in 16 time slots (each slot being 1.25ms). The small digits are lit in time slots 0 through 7, and the large digits alternate back and forth during time slots 8 through 15.

The computer can read the selected switch bank by reading from tri-state driver Z16 (using the $\overline{\text{RD SWB}}$ strobe). To guarantee that the switches can be read correctly, the computer only reads the switches in the brief intervals between the illumination of each display digit. The sequence, which only takes a few microseconds, consists of turning off the display (writing 0 to Z15), selecting the next digit and switch bank (writing to Z17), inputting the switch bank data (reading from Z16), and turning on the next digit (writing to Z15). The firmware compares each switch bank reading with a memory image of what the bank looked like last time it was read. This allows the computer to detect the initial depression of a switch independent of how long it is held.

8. CASSETTE INPUT/OUTPUT (sheet 2)

The square waves generated by the computer (TAPE OUT) are attenuated by R21 and R20 to a level suitable for feeding into a microphone jack on a cheap cassette recorder. The signal that comes back from the earphone output of the recorder during playback is much stronger, but only vaguely resembles the original signal and must be squared up again. Comparator Z8 performs this. Note the large amount of positive feedback necessary to clean up the signal. The D-flip-flop (Z10A) synchronizes the signal to the 2MHz clock (so that it will work correctly with the timer) and provides the necessary complementary versions of the signal for detecting positive and negative edges.

9. CASSETTE MOTOR SENSE/CONTROL (sheet 2)

This circuit uses a dual opto-isolator to isolate the Chroma circuitry from the voltages used to drive the cassette motor. When the MOT OUT signal is driven high, opto Z9A turns on, which, if there is any voltage in the motor circuit, turns Q2 on, allowing the motor to run. There will be a significant drop between MOTOR+ and MOTOR-, due to the Vbe drop of Q2, the diode drop of CR30, and the saturation drop of the transistor in Z9A. But this voltage is what allows the other half of the circuit to sense the state of the cassette recorder controls. If the cassette is set to STOP (or there is no cassette connected), obviously there will be no voltage on the MOTOR lines. Thus, opto Z9B will be off, and Q3 will be off, and MOT IN will be high. If the cassette recorder is turned on, but the Chroma's control of the cassette (Q2) is off, the full motor voltage (usually 6 volts or so) will appear across opto Z9B and FET Q10. The FET functions as a resistor, allowing enough current to flow to turn on the opto and Q3 and pull down MOT IN, but not enough for the motor to turn. If the Chroma computer decides to let the cassette run, it turns on Q2, but there is still enough of a voltage drop across the circuit to turn on opto Z9B and hold MOT IN down. This is because the FET acts as a nonlinear resistor, with a lower resistance at lower voltages (nearly a constant current sink). This arrangement allows the computer to sense whether the cassette controls are on or off, independent of whether the Chroma is allowing the cassette to actually run.

Diode CR31 is there to protect against inductive kickback when the motor is turned off. Capacitor C6 is there to slow the rise of MOT IN way down. This is necessary because a cassette recorder operated from

AC with no batteries installed usually runs its motor off unfiltered rectified AC. Were it not for C6, the MOT IN line would toggle 120 times a second.

10. LED DRIVERS (sheet 2)

The sixteen LEDs on the panel are driven from two latches (Z5 and Z6) that can be written into using the WR LEDS and WR LEDS+1 strobes. Using LS latches as current sources directly driving the LEDs (with only the internal latch resistance to limit the current) yielded a reasonable brightness, without wasting board space for 16 resistors. All blinking of the LEDs is performed by the computer. Z5 is only strobed when a panel switch is pressed. Z6 is strobed several times a second, as it drives the LEDs that must flash.

11. TAPPER DRIVER (sheet 1)

Since membrane switches provide no tactile feedback, a solenoid tapper is provided in the Chroma. Whenever the WR TAP strobe is activated, flip-flop Z38A is set. This turns on Q1 and applies a hefty current from the unregulated power supply to the solenoid. Rather than have the computer turn the transistor off 20ms later (that's about 3 months in computer time), a feedback network is provided that makes the flip-flop function as a crude one-shot. R52 provides the negative feedback that ultimately resets the flip-flop. Capacitor C20 provides the time constant. And connecting the other side of C20 to the opposite output of the flip-flop (rather than to ground) provides some positive feedback to make sure that the switching is clean. Diode CR23 protects against inductive kickback when the solenoid shuts off.

Obviously, there is no direct connection between the panel switches and the tapper circuit. Instead, pressing a switch causes the computer to execute a certain part of its program that handles the appropriate switch function. One of the instructions in each switch handler is an instruction that writes to the memory location that corresponds to the tapper, activating the WR TAP strobe. The tapper can be disabled from the panel, but this is not done electrically. Rather, the location that the computer writes to is changed so that the tapper won't be triggered.

12. MISCELLANEOUS INPUT/OUTPUT (sheet 1)

There is a 6-bit output port (Z30) that is strobed by WR PRSS. This latch is used to select one of the 64 keys on the keyboard and deliver the voltage from its pressure sensor to the PRESS input on the A/D converter. There is also an output port strobed by WR MSCO that contains miscellaneous output bits. Latch Z29 is activated by this strobe, and drives the three interrupt masks, the cassette data output and the cassette motor control. The same strobe also goes to the Channel Mother Board, where two more bits are latched from the B0 and B1 data bus bits. When the computer strobes RD MSCI, it reads in eight miscellaneous input bits, including the state of the external computer interface ports, the timer, the cassette motor sense, the LOCK switch on the rear panel, and the three footswitches. There are also three other strobes that go to the Channel Mother Board via Z41. The WR SHA strobe is used to write a sample-and-hold address into a latch. The WR SYND strobe is used to write 6 bits of data destined for one of the synthesizer channels into a buffer latch. The WR SYNA strobe is used to transfer the contents of the buffer latch into any of the 24 latches on the individual channel boards.

DUAL CHANNEL BOARD CIRCUIT DESCRIPTION

Each Dual Channel Board in the Chroma consists of the following sections, as outlined in the schematic:

1. Sample and hold bank
2. Data latches
3. Oscillators (A and B)
4. Filters (A and B)
5. Amplifiers (A and B)

Each section will be covered individually in the following descriptions, except that the B channel circuits will only be described as they differ from the A channel.

1. SAMPLE AND HOLD BANK (sheet 2)

This circuit consists of eight sample and holds and their associated switching logic. These sample and holds each employ two holding capacitors separated by a resistor, allowing the output voltage produced to be filtered, avoiding sudden step changes. A particular output is set to a voltage by applying the desired voltage to the DAC input, putting the appropriate sample and hold address code on the three SHA lines, and bringing SHEN low to enable the selected sample and hold. This causes one of the channels in Z19, a 4051 CMOS switch, to turn on, connecting the DAC voltage to one of the 0.033uf capacitors. This voltage doesn't immediately appear at the corresponding op-amp output, as it must first go through a low-pass network consisting of a 1M resistor and 0.0068uf capacitor. This slows down the sudden transition that could be caused if the current sample is different from the previous sample applied to this channel. The Chroma computer enables each sample and hold about 50 times a second. The filtration due to the resistor and second capacitor in each channel allows the Chroma to generate rapid portamentos and envelopes without the listener being able to hear that they are comprised only of a few discrete steps.

It is often necessary for the computer to change a particular voltage instantly. This is used for pitch changes without portamento, envelopes with sharp attacks, and trills. The computer can cause any individual sample and hold to produce a sudden, unfiltered, change in output voltage by merely bringing the FAST line low during the sample period. Z25B functions, in this circuit, like an OR gate: if FAST is low and SHEN is low, Z20's enable line will also be low. Thus, there will be a switch turned on in both Z19 and in Z20, connecting the DAC voltage to both capacitors

in the selected sample and hold. Since both capacitors are thus charged to the desired voltage, there will be no filtering effect on the control signal.

The computer leaves each sample and hold selected while it calculates the voltage level to be sent to the next sample and hold. This allows somewhere between 150us and 500us for each sample and hold to acquire the DAC voltage. There are 64 sample and holds in the Chroma, and they are sampled in order of board number, board 0 first, and, on each board, in the order that they appear in the schematic, producing the PITCH A signal first and the VOLUME B signal last.

2. DATA LATCHES

There is a 6-bit data "bus" that connects to all the Dual Channel Boards. This bus is not the same as the main system data bus, as the bus is too noisy to bring up onto the channel boards. This 6-bit bus is loaded with data by the computer whenever it wants to set any of the data latches on any channel board. Once the data is set up, either the $\overline{\text{STB0}}$, $\overline{\text{STB1}}$ or $\overline{\text{STB2}}$ line will be given a pulse, writing into the appropriate latch. Most of the latch bits connect directly to various places within the channel circuits. The two leftmost bits are decoded to produce an active-low level on one (or none) of three lines, $\overline{\text{SYNC}}$, $\overline{\text{RING MOD}}$ or $\overline{\text{FILT FM}}$.

The $\overline{\text{SYNC}}$, $\overline{\text{RING MOD}}$, $\overline{\text{FILT FM}}$ and PATCH bits are updated whenever the Patch parameter is changed. The OUT bits are updated whenever the Output Select parameter is changed. The WAVE, MODE and RES bits similarly correspond to the Wave Shape, Filter LP/HP and Resonance parameters. If the Patch parameter is 0 in the program that is controlling a particular board, the 0 and 1 latches (Z28 and Z27) will both be controlled by the same "A" parameters. If the Patch parameter is non-zero, the A and B channels are controlled independently.

3. OSCILLATORS (sheet 1)

EXPO CONVERTER. Z1 and Z4, and associated Rs and Cs form two identical garden-variety expo converters. They accept linear control voltages (from the PITCH A and B sample and holds) in the range of 0 to 5 volts and produce an exponentially controlled current ranging from 120uA down to about 100nA. These circuits have negative control, meaning that the highest oscillator pitch is attained at the lowest control voltage. The scaling is such that the output current (Z1-1 or Z1-11) changes by a factor of 2 (and the pitch changes by an octave) as the control voltage changes by slightly less than 0.5 volts. Thus, the oscillator has a typical range of somewhat more than ten octaves.

CHARGE PUMP OSCILLATOR. The design of the oscillators themselves is unconventional in the domain of electronic music, but have been around in the field of data acquisition for years. They are called "charge pump voltage-to-frequency" converters. The basic oscillating element is a 4151. It consists of a comparator, a one-shot, and a switched precision current source. Basically, the current from the expo converter is integrated by op-amp Z5 and capacitor C3 (or C4), causing the op-amp output voltage to ramp upwards at a rate proportional to the control current. Pins 6 and 7 on the 4152 are the comparator inputs. When the op-amp output, which drives pin 7, reaches 5 volts, the voltage on pin 6, the one-shot inside the 4151 is triggered. So far this is just like any other synthesizer oscillator; but most synthesizer oscillators use the one-shot output to essentially short circuit the integrating capacitor, forcing the output back to zero. Ideally, this discharge, or retrace, should happen instantly, as it is not "taken into account" by the circuit in determining the rate of oscillation. Unfortunately, it is never instantaneous, and at high frequencies this retrace time can appreciably lengthen each cycle, causing the characteristic "high-end droop" that most synthesizer oscillators have compensating adjustments for.

A charge pump oscillator does not use the one-shot to force the integrating capacitor back to zero volts, but rather uses the one-shot to pump a fixed quantum of charge into the capacitor in the opposite direction than the steady current from the expo converter. This fixed charge is created by turning on a constant current source for a fixed amount of time. In this circuit, the one-shot time is quite long compared to other synthesizer oscillator retrace circuits, about 20us. This is acceptable because the retrace time is inherently perfectly compensated for. At low frequencies, the charge pump (which, by the way, comes out pin 1 of the 4051) is adjusted by means of a trim to kick the integrating capacitor voltage back to exactly zero volts. At high frequencies, this charge is "working against" higher currents from the expo converter, and so the retrace, which is allowed the same amount of time, doesn't kick the capacitor voltage all the way back to ground. This compensates for the extra time spent retracing.

> The linearity of this circuit can be easily proven by reasoning that the total current from the expo converter during each cycle must exactly counterbalance the total current from the charge pump during each cycle. If it didn't, the integration in each cycle would not wind up at the same 5 volt level. Thus, the following identity holds:
>
> $$I_{expo} \times t_{cycle} = I_{pump} \times t_{pump}$$
>
> Since the frequency is the reciprocal of time:
>
> $$f = \frac{1}{t_{cycle}} = I_{expo.} \times \frac{1}{I_{pump} \times t_{pump}}$$
>
> In other words, f is proportional to $I_{expo.}$ Look at it on an oscilloscope if you can't visualize it.

The output of the oscillator on Z5 pin 1 (or pin 7) is a sawtooth whose retrace is rather slow compared to most synthesizer oscillators. Pin 3 on the 4151 is an

open collector that turns on during this retrace period. Thus the voltage on the right side of R17 (or R18) is a sawtooth with a very fast retrace.

SYNC CIRCUIT The B oscillator differs from the A in that it is provided with a method for hard synchronization. The three discrete transistors, Q1, 2 and 3 provide this function. Whenever the A oscillator's cycle completes, its sawtooth output snaps from 5 volts back to ground. This sudden transition is differentiated by C19 and R79 and fed as a very narrow pulse through Q1 to the base of Q3. When this occurs, Q3 shorts out integrating capacitor C4, resetting oscillator B to the start of its cycle. If, however, the SYNC control line from the data latch is high, Q2 will be saturated on, its collector will be at about 0.7 volts, and the tiny pulse will be absorbed without passing through Q1. Resistor R81 keeps Q3 solidly off except during synchronizing pulses.

PULSE COMPARATOR Resistors R19 (or R20) and R21 (or R22) mix the sawtooth produced by the oscillator with the pulse width control voltage from WIDTH A (or B) sample and hold. This signal is compared to a fixed 2.5V reference by comparator Z6. (The feedback components are simply to prevent oscillations at the transition point.) Since the sawtooth and the pulse width control voltage are both 0 to 5 volt signals, the input to the comparator on pin 2 (or 6) will be a 2.5Vp-p sawtooth whose average level can be adjusted from 1.25V to 3.75V. Thus, the comparator output will be a pulse whose duty cycle is variable across the entire range from 0 to 100%.

WAVE SHAPE SELECTOR CMOS switch Z8 (or Z9) selects one of four wave shapes. The upper two are, obviously, the pink and white noise signals that are produced on the Channel Mother Board. The lower two inputs select oscillator signals. Pin 5 is provided with a combination of the pulse signal, the pulse width control voltage and a fixed bias that yields a pulse signal that has no DC component. As the pulse width is varied, the pulse width control voltage raises and lowers the signal keeping its average DC level at zero volts. Pin 1 of the CMOS switch gets a combinaton of the pulse, the pulse width control voltage, a fixed bias and the sawtooth. This produces a mix that is indistinguishable from two sawteeth. If you can't visualize this, set the Wave Shape parameter (No. 33) to 0 and look at the output of Z10 while varying the Width parameter (No. 34). This signal is also DC free. The A oscillator differs from the B in that its output signal can be replaced with a ring modulator signal when the RING MOD line from the data latch is low. The four NAND gates perform a digital exclusive-or function on the pulse signals from the two oscillators. This produces a perfect ring mod signal if the inputs are square waves, and a reasonable ring mod effect if the inputs aren't square. Z10 buffers whatever wave shapes are selected. Note: the signals at the inputs to the CMOS switches disappear when you select them, because they are connected through the switch to the summing junction of Z10. In other words, the CMOS switches are used as current switches.

4. FILTERS

The filters are implemented using Doug Curtis' dual state-variable filter chips. A complete analysis of these chips will not be attempted here, but this is basically what occurs in the circuit. Z11 is a CMOS switch, common to both filters, that determines, under control of the Patch parmeter, what signals feed the filters. These switches operate in the current mode, as they feed the singal into a 10 ohm resistor R57 (or R58). Thus the signal that appears on pin 3 (or 13) of the CMOS switch is very small, typically 50mV p-p. The filter chip requires signals that small to avoid distortion. The output amplifier, which brings the signal level back up to normal, consists of op-amp Z14 and associated resistors. This circuit provides differential gain, and blocking capacitor C13 (or C14) assures that the offset voltages in the filter chip are not amplified as well. The filter is basically connected as a high-pass filter, where the signal is applied to the lower end of C9 (or C10) and taken off the upper end of the same capacitor. The filter chip, in this case, looks like a shunt inductance and resistance to ground. If CMOS switch Z12B (or Z12C) is switched to ground, this is all the circuit does, and the output buffer provides single ended gain. If the switch is switched the other way, the input signal is delivered to the IN 2 pin on the chip, which is a band-pass input, and to the inverting input of the output buffer. The OUT 1 line thus produces a combination of a band-pass and high-pass response which, when combined out of phase with the input signal, yields a low-pass response. Remember, low-pass + band-pass + high-pass = everything. This configuration was chosen because it has few parts, and because it can perform switching between the low-pass and high-pass function without generating a DC transient.

The three feedback resistors, R69, 71 and 73 (or R70, 72 and 74) provide a tiny amount of positive feedback around the filter that, when the resonance is raised far enough, causes the filter to oscillate. The parallel NPN/PNP transistors counter this effect with negative feedback when the output signal reaches about +3V. This prevents the filter from hard clipping at high resonance levels, providing instead a soft "rounded" distortion.

The F terminals on the filter chip are the inputs to the on-chip expo converters that control the tuning of the filter. Like the oscillator expo converters, these provide negative control. Resistors R5 and R45 (or R6 and R46) scale these inputs at slightly under 0.5V/octave, just like the oscillator. The Q terminals provide negative exponential control of the resonance of the filters. The three resonance control bits from the data latch for each channel are used to encode the setting of the Resonance parameter. When the parameter is 0, the three bits are all logic 1 (5 volts), and when the parameter is 7, the three bits are all at zero. Resistors R47, 49 and 51 (or R48, 50 and 52) combine these in a binary weighted manner. The purpose of the transistor is to provide a resonance boost when the parameter is set to 7. Normally (that is, when the filter

isn't being used as an oscillator) at least one of the resonance control bits is high. This turns the transistor on hard, so that the current that flows into the 100 ohm summing resistor R53 (or R54) is thus equal to the sum of the control currents fed into the base of the transistor and the current through the 33K resistor on the collector. As the resonance parameter is increased, less current flows through the base, but the transistor remains saturated. When the resonance parameter makes the final transition from 6 to 7 and all three bits go low, the transistor shuts off and the current through the emmitter drops sharply to zero, causing a large increase in Q. This guarantees that all filters will oscillate when set to 7, but not when set to 6. The added 33K resistor (R115 or R116) causes the resonance to be increased slightly at higher frequencies, to overcome a slight reluctance to oscillate.

Op-amp Z29A isn't really part of the filter at all, and should have been drawn someplace else. It's a current inverter. Op-amp Z29B is connected in the rather unconventional "left-facing ground buffer" configuration. Unfortunately, the theory behind this circuit is beyond the scope of this document. Suffice to say that it works perfectly.

5. AMPLIFIERS

CMOS switch Z15 (common to both amplifiers) selects a signal to be controlled and feeds it, as a current, into the low impedance (summing junction) input of the VCA chip Z16. The output of this chip is also a current (The output stage of the chip is similar to that of a 3080 OTA chip). The control voltage from the VOLUME A (or B) sample and hold is attenuated to the required 0 to 3V level and applied to the chip's linear control input. The 0.1uf capacitor on this input slows the control voltage changes down just enough to make a sharp attack or release sound like a soft pop and not a sharp tick. The A amplifier's output current is routed to one of the four summing busses in the Channel Mother Board by Z17. The B amplifier's output current is routed to one of three places. If the Patch parameter selects filter FM, this signal current is fed into the frequency control input of the A filter. If the Patch parameter selects the series or parallel filter configuration without filter FM, the signal current is fed back and mixed with the A oscillator. Otherwise, the signal current is mixed into the output. The rest of the signal routing on board is tedious but simple and is easily traced with the help of the Patch parameter diagrams in the Chroma Programming Manual.

CHANNEL MOTHER BOARD CIRCUIT DESCRIPTION

The Channel Mother Board consists of the following circuits, as outlined on the schematic:

1. Sample and hold decoder
2. Data latch
3. Data strobe decoder
4. Oscillator and output mute latch
5. Noise generator
6. Output summing amps
7. Zero crossing detector

Each section will be covered individually in the following descriptions.

1. SAMPLE AND HOLD DECODER

This circuit is used to selectively enable one of the 64 sample and hold circuits on the channel boards. Z1 and Z2 form an 8-bit latch that can be written to by the main computer using strobe $\overline{\text{WR SHA}}$. The low order six bits address the sample and hold, bit 6 is an active low enable signal, and bit 7 is the active low "fast" signal described in the Dual Channel Board Circuit Description. The upper half of the sample and hold address (from data bus bits B3, B4 and B5) are decoded by Z7A, Z7B and Z8. These three bits appear on Z2-2, Z1-10 and Z1-7, and the last bit also appears complemented on Z1-6. The two OR gates and the two one-of-four decoders function as a one-of-eight decorder, enabled by Z1-15. The three low-order bits of the sample and hold address (from Z2-10, -7 and-15) are decoded on the channel boards themselves.

The firmware always manipulates the sample and hold latch in the same three steps. First, it turns off the current sample and hold by writing the sample and hold number to this port with bit 6 (the enable bit) inactive (high). Second, it selects the next sample and hold by writing the new sample and hold number to this port with bit 6 still high. The "fast" bit, bit 7, will be set as necessary and the DAC output voltage will be changed at this time. Third, the sample and hold is enabled by repeating the last operation with bit 6 low. This entire sequence takes approximately 10us and eliminates any possible glitches that might disturb other sample and holds.

Each sample and hold is left selected for at least 100us while the computer does other work. Thus, the enable bit, Z1-15 will be active (low) most of the time. Each of the sample and hold address bits will look remotely like a square wave, as each sample and hold is addressed in a squence, from 0 to 63. This sequence is disturbed every time a new note is struck.

2. DATA LATCH

The main computer sends digital control signals to each board in a two-step process. First, a 6-bit word is written to the data latch using strobe $\overline{\text{WR SYND}}$. Second, the data strobe decoder (explained below) is used to transfer the data to the desired latch on any of the channel boards.

3. DATA STROBE DECORDER

Once a word is set up in the data latch, it can be copied into any of the latches on the individual channel boards by writing the number of the latch using the $\overline{\text{WR SYNA}}$ strobe. Each channel board has three latches, and therefore has three strobes for triggering them. A fourth strobe to each board is provided for future expansion. Thus, there are 32 total strobes that must be individually controllable by the main computer. Latch Z5 and the right half of flip-flop Z4 form a 5-bit

latch to which can be written a five bit address code. The left side of flip-flop Z4 is configured as a crude one-shot by connecting its output through a lag network back into its reset input. Whenever one of the channel board latches is to be strobed, the WR SYNA strobe (which is an active low pulse) will trigger this one-shot on its trailing (rising) edge. Z7C, Z7D and Z9 form a one-of-eight decoder that routes this one-shot pulse according to the lowest 3 bits in the latch number. (These 3 bits come from data bus bits B0, B1 and B2, and appear on Z5-15, Z5-2 and Z4-1, and the last bit also appears inverted on Z4-2). Each of the eight lines coming out of decoder Z9 corresponds to one of the dual channel boards. The strobe pulse is further routed to one of the four strobe lines on the selected channel board by one of the one-of-four decoders Z10A through Z13B. (The bits that select which of the four strobes to activate are the upper two bits in the latch number. These bits come from data bus bits B3 and B4 and appear on Z5-10 and Z5-7.)

4. OSCILLATOR AND OUTPUT MUTE LATCH

Whenever the main computer does a write operation using the WR MSCO strobe, the upper six bits of the data bus are latched on the I/O board and the lower two bits of the data bus are latched by Z6 on this board. All the bits in this "port" are miscellaneous in nature. The two that appear here are mute bits. The low order bit, which appears on Z6 pin 13 (and inverted on Z6 pin 12) is used as an output mute. The next bit, which appears on Z6 pin 1, is used as an oscillator mute bit. It disables the audio input to each filter on the Dual Channel Boards.

5. NOISE GENERATOR

Two digital noise generator chips, Z14 and Z15, are employed in this circuit. Each chip has its own on-chip clock and a shift-register type noise generator that generates a pseudo-random sequence of 0s and 1s at 12 volt logic levels. Since the two chips run asynchronously, the pseudo-randomness is turned into something truly random and free of repetition. By itself, a random stream of bits sounds like white noise. This signal is buffered and attenuated and delivered to J5 pin 6 on each Dual Channel Board. The noise generator output is also filtered by a network that approximates a 3db per octave rolloff, yielding pink noise. This signal is buffered and delivered to J5 pin 8 on each Dual Channel Board.

6. OUTPUT SUMMING AMPS

The signal currents from each of the Dual Channel Boards are mixed using four summing busses, SUM 0 through SUM 3. CMOS switches Z16 and Z17 route these currents into summing amps Z18 and Z19, or divert them, under control of the output mute bit. The voltage outputs are roughly line level signals, and are sent to the EQ Board.

7. ZERO CROSSING DETECTOR

When the outputs are muted, as during auto-tune, the signal current from SUM 0 summing bus is fed into comparator Z20. This comparator "squares up" the signal and feeds it to the I/O Board for measurement. During filter tuning, the signal being processed is a sine wave, and so some positive feedback is utilized (through R11) to keep the comparator from oscillating as the signal slowly passes through zero. The two diodes clamp the input to the comparator. The negative clamp uses a germanium diode for its lower forward drop. The intent here is to protect Z16 pin 4 from excessive voltages.

POWER SUPPLY

The power supply consists of the following circuits:

1. Primary and transformer
2. Analog 5V regulator
3. Analog 12V regulator
4. Analog -12V regulator
5. Digital 5V regulator
6. Digital 5V preregulator
7. Reset cirucit

Each will be covered individually in the following descriptions.

1. PRIMARY AND TRANSFORMER

The power transformer in the Chroma is a dual primary design. The DPDT line voltage selection switch S1 is used to connect the two identical primaries in parallel for operation at 120VAC, or in series for operation at 220VAC. R1 and R2 are metal-oxide varistors which act as a low impedance clamp at voltages above those expected from the power line. This prevents high voltage transients from entering the unit. The rear panel power connector includes an RFI filter to further isolate the inside and outside of the instrument from each other.

The transformer has only one secondary winding with a grounded center tap. All voltages in the system ultimately come from one of three full-wave rectifiers connected to this winding. CR1 and 2 (the large rectifiers on the board) provide power to the digital preregulator and regulator. CR6 and 7 provide power to the positive analog regulators. CR8 and 9 power the negative analog regulator.

2. ANALOG 5V REGULATOR

This regulator takes its input from filter capacitor C7, which has somewhere between 16 and 33 volts on it, and generates a very stable, but not particularly powerful, 5 volt reference. Op-amp Z1A and transistor Q6 make up the active part of the regulator. Resistor R19 sets the current limit at roughly 250mA. Z3, though it behaves like a zener diode, is actually an IC reference that has a very low dynamic impedance and temperature coefficient. It establishes pin 2 of the op-amp at 1.2 volts below the output voltage of the circuit. R17 and R20 control the gain of the circuit, and R21 and trimmer R22 allow the ouput to be set at exactly 5.000V. R42 is only there to make sure that the circuit starts up correctly.

3. ANALOG 12V REGULATOR

Taking its input from the same filter capacitor, this circuit amplifies the 5V reference and produces 12V at up to about 700mA. Op-amp Z2A and transistor Q7 make up the active part of the regulator, R23 and R24 set the gain at 12/5, and Q8, R25 and R26 provide current limiting.

4. ANALOG -12V REGULATOR

This circuit takes its input from filter capacitor C11 and its reference from the output of the 12V regulator. Op-amp Z2B is connected as a unity gain inverting amplifier (R27 and R28 set the gain). Its output, which can only go as low as ground, drives cascode transistor Q11, which in turn drives pass transistor Q9. The current limiting circuit is slightly "upside-down" due to the fact that the pass transistor inverts. R31 sets the limit at about 700mA, and when this is exceeed current is diverted from the input of the cascode transistor. Diode CR13 is only there to protect the input of the op-amp from negative voltages.

5. DIGITAL 5V REGULATOR

This circuit, based around op-amp Z1B and power MOSFET Q4, acts as a voltage follower, boosting the available current to several amps. A MOSFET was chosen because of its high input impedance and its ability to operate with only a few tenths of a volt across it. At high currents, the resistor in a conventional current limiting circuit begins to dissipate appreciable current because it can have up to 0.7V across it. This circuit uses differential sensing to reduce the voltage across sense resistor R12. The 12K and 120 ohm resistors (R13 and R15) are driven with 5V between them, while the 910 ohm and 6.8 ohm resistors (R11 and R14) see between them whatever the current sensing voltage is. This extra bias means that the current sense resistor only need have about a quarter of a volt across it to start current limiting. The difference in ratio between R13/R11 and R15/R14 results in a foldback limiting characteristic as well.

6. DIGITAL 5V PREREGULATOR

The 5V regulator takes its input from the large filter capacitor C3. To keep the dissipation in the regulator down, this voltage is preregulated to about 6V. In fact, there is a crowbar-type overvoltage protector (Z4) mounted right across the filter capacitor terminals that makes sure this voltage doesn't get much higher than 7V. The preregulator takes its input from the secondary through CR1 and CR2, but no filtering is performed prior to the preregulator. Instead, the preregulator functions as a switch that turns on and off at the 120Hz rectified line voltage rate.

The switch consists of power transistor Q1 (the TO-3 package) driven by power MOSFET Q2. This combination was chosen beacuse of its low on voltage (not much more than a volt) at high currents (20A pulses are found in this circuit). The gate of the MOSFET is normally pulled up to the unregulated plus supply voltage by R6 (through R4), meaning that the switch is normally on. As the power line voltage rises during any particular half-cycle, a point is reached where the switch becomes forward biased. At this point, filter capacitor C3 starts to charge. If you look at the junction of CR1 and CR2 with a scope, you should see the voltage rising to about 7V and then leveling off when hit with the heavy load of the filter capacitor. As soon as the filter capacitor is charged sufficiently to run the 5V regulator, the switch is turned off. This appears as the sudden rise in the rectifier output voltage. Thus, the rectifier output looks like a conventional full-wave rectifed sine wave with a triangular "bite" taken out of it during its rise by the temporary connection to the large filter capacitor. When the switch turns off, the transformer secondary voltage continues on up in voltage to where it charges the analog supply filter capacitors, C7 and C11.

The rest of the preregulator circuit is involved with determining when in each cycle to turn off the switch. Transistor Q3 senses (through R3 and R7) when the rectifier voltage gets a few volts above the final output voltage. When it does, it starts to turn off the switch circuit. The sudden removal of the load causes the voltage being sensed to rise sharply. Thus there is positive feedback in the circuit, assuring that the switching will occur quickly. The emitter of the sense transistor Q3 is connected to the top of the current sensing resistor R12 and not to the output in order to allow for its voltage drop. Resistor R7 is connected to the bottom of the current sense resistor, causing the drop across the resistor to be overcompensated for, which allows for the resistance of, and voltage drop in, pass transistor Q4 at higher output currents. The trimmer R46 allows the trip point of this circuit to be adjusted.

Note that the preregulator is referenced to the digital 5V output, and not to some absolute reference. Under normal operation, the preregulator will be putting out about 6VDC, with .5 volts of ripple, and the regulator will be cutting that down to a smooth 5V. If the output is shorted, the preregulator voltage will automatically come down to about 1V, maintaining a constant drop across pass transistor Q4. This keeps the power dissipation down under short-circuit conditions.

7. RESET CIRCUIT

In any computer system, there is a need for a system RESET signal that remains active until the power supply is fully stabilized and the processor clock has run for a bit. This is usually attained with a simple RC network. But in a computer system that employs non-volatile RAM, the RESET signal must also be asserted again before the supply drops out of regulation when the power is shut off. If this requirement isn't met, the computer can produce spurious signals when the supply falls below 4.75V, damaging the integrity of its own memory. In order to sense power failure "before it happens," it is necessary to create a

filtered version of the rectified line voltage that has a faster "droop" than that of the main filter capacitor, C3. Capacitor C10 performs this function. C10 takes its charge from the same rectifiers as the analog positive supplies, but is isolated from filter capacitor C7 by the extra diode, CR10. C10 is pulled down, not to ground, but toward the opposite supply by R40 (CR16 prevents this voltage from ever actually going negative). Thus, the voltage on C10 will be a crude, rounded, sawtooth at 120Hz, that charges up to 25V or so and then droops sharply. R39 and C12 form a low-pass filter, or would if it weren't for CR15. During power up, C10 shows its characteristic sawtooth, and C12 shows a gradual rise in voltage towards the DC level of the sawtooth. CR15 keeps this voltage from getting any higher than the negative-most extreme of the sawtooth. During power-down, the sawtooth stops abruptly and CR15 quickly pulls the voltage on C12 back to ground, before the supply has a chance to come out of regulation.

R38 couples this signal into the Schmitt trigger circuit consisting of Q12 and Q13. This circuit "squares up" the very slow rise of C12's voltage during power-up, and its rather slow fall during power-down. Note the positive feedback loop in this circuit. The voltage on C12 has to rise to about 5V before the circuit switches on. Then, the voltage on C12 has to drop to about 4V before it switches off again. Zener diode CR14 opens up the loop and forces $\overline{\text{RESET}}$ active if the digital 5V supply (which powers this circuit) falls out of regulation.

EQ BOARD

The EQ Board consists of the following circuits, as outlined on the schematic:

1. Volume and ground isolation
2. Custom equalization
3. Audio mixer and mute
4. Tone controls
5. Balanced output amplifiers

Each will be covered individually in the following descriptions.

1. VOLUME AND GROUND ISOLATION

This circuit controls the volume of the signals from the quad outputs of the Channel Mother Board. The VCA chips that are used are the same as those used in the channels themselves. The input terminals look like summing junctions and are thus fed through resistors. The outputs are currents that are converted to voltages by op-amps Z3 and Z4. Note that the VCA chips are the only circuits on the board that are referenced to the normal ground line from the power supply. Though not shown on the schematic, this line actually comes from the Channel Mother Board along with the quad audio signals. All the remaining circuits are referenced to the OUTPUT GND line which comes directly from the rear panel. If any differential voltage exists between these two grounds, it will not affect the signal, as the signal is passed in the form of a current from the high output impedance of the VCAs to the low input impedance of the op-amps.

The control voltage inputs on the VCA chips are all tied in parallel and driven by the VOLUME potentiometer R5. The control voltage inputs have a linear transfer function and expect voltages from 0 to about 2 volts. R6 and R7 divide the slider voltage down to this level, and incidentally make the apparent taper of the volume control a little more "audio" by loading down the slider when it is set near middle.

Note that the cassette audio signal is mixed in with the 0 channel. This allows easy cueing of tapes by ear, without having to unplug the earphone jack on the cassette recorder. Note also that the VCAs are powered from a heavily filtered 4.3V supply shown on the right side of the schematic. It is derived from the analog +5V reference to the TUNE slider, and is intended to reduce noise coupled into the VCAs.

2. CUSTOM EQUALIZATION

No circuits are actually installed for this function, but there are solder pads on the board for possible installation of fixed equalization modules in channels 1, 2 and 3. The quad outputs are wired up to stereo phone jacks that function as combination send/receive jacks. The tip of each jack is driven with the (unequalized) output signal. The ring can be used as an input to the final mono mix. If a plug is not inserted into the jack, the ring is driven (via the ring shunt) with the equalized output signal. Thus, using a jack as a send/receive connector causes any internal custom EQ to be bypassed. If the jack is left empty, the custom EQ for that channel remains in the circuit, and may be selected using the Output Select parameter.

Channel 0 has no provision for custom EQ.

3. AUDIO MIXER AND MUTE

The quad outputs (or the signals fed in on the rings of the four outputs jacks) are mixed in this circuit. JFET Q1 and CR1 form an analog switch that interrupts the signal during system $\overline{\text{RESET}}$ (power-up and power-down). R25 and R26 level shift the $\overline{\text{RESET}}$ signal, as the JFET expects a negative control voltage. C17 is necessary to filter any computer noise from this line.

4. TONE CONTROLS

This is an ordinary three-band tone control circuit. C10 and C11 "short out" the BASS control at high frequencies, allowing it to affect the response only at low frequencies. C15 "disconnects" the TREBLE control from the op-amp at low frequencies, allowing it to affect the response only at high frequencies. The MIDDLE control uses a combination of the two effects.

5. BALANCED OUTPUTS

These two circuits are simple power amplifiers using op-amps Z6A and Z6B as voltage followers. Increased current output capability is provided by the NPN/PNP output stage added inside each feedback loop. The diodes and 22 ohm resistors make the transistors operate class AB.

STACK SWITCH BOARDS

The Right Stack Switch Board contains the following circuits, as outlined on the schematic:

1. Bank select decoder
2. Switch banks
3. Sense amps

The Left Stack Switch Board is an extension of the Right Stack Switch Board and has the same circuits minus the sense amps. These circuits will be covered individually in the following descriptions. The term "stack switch" comes from the way each switch is assembled as a stack of different layers.

1. BANK SELECT DECODER

When the keyboard scanning computer on the I/O Board wants to read the state of a bank of eight key-switches, it addresses the bank by putting one of 16 binary numbers on the KA lines. These lines drive the bank select decoders (Z1) on each board (KA2 is inverted on the right board), causing exactly one of the 16 decoder outputs to be activated. These outputs are open-collectors, and, when activated, connect a row of eight switch contacts to ground.

2. SWITCH BANKS

Each keyswitch has a lower, normally closed, contact called the A contact, an upper, normally open, contact called the B contact, and a center wiper contact that is moved by the key. The keyboard has 64 keys which are grouped into eight banks of eight keys each. Half of these banks are handled by each Stack Switch Board. The keyboard scanning computer reads the state of a bank of A contacts or a bank of B contacts by connecting the row of contacts to ground. All the wiper contacts connect, through resistor packs, to the keyboard bus KB0 through KB7. This is a current summing bus, and any closed contacts in the selected bank will cause 500uA to be sinked from the appropriate line on the bus.

3. SENSE AMPS

The keyboard bus is pulled up to the +5V rail by the 100 ohm resistors in Z6. A closed contact in the selected switch bank will pull 500uA from a bus line, which will pull it, and one of the comparator (Z7 and Z8) inputs, down 50mV. The other inputs on the eight comparators are connected to a constant voltage that is about 25mV below the +5V rail. Thus, each comparator resolves the state of one switch in the selected bank and produces a standard 5V logic level on one of the keyboard data lines KD0 through KD7. Each data line that goes back to the keyboard scanning computer will be a 0 if the corresponding switch contact is open or a 1 if it is closed.

The sense amps are powered from the +12V supply.

SECTION 3. DISASSEMBLY

Access to the Chroma for troubleshooting is quite straightforward. Figure 3 - 1 shows an exploded view of the screws holding the top cover in place. Remove the nine black screws (1-9) from the back and the four bronze screws (11-14) from the wood rail above the control panel. Do not remove screw 10 until you gently remove the cover. Screw 10 holds a green ground strap under a nut inside the cover (see Figure 3 - 2) which may be removed after you lift off the cover.

Remove four screws (15-18) from the sloping panel (Figure 3 - 2). The panel is pivoted and may be raised up and back as shown in Figure 3 - 3.

As can be seen from Figure 3 - 3, most electronic boards are easily accessible with the Chroma open. Notice the order of the Dual Channel Boards. They are numbered from left to right in a "U" shaped configuration, while facing the keyboard. These numbers are silkscreened on the Channel Mother Board (not shown) into which the Dual Channel Boards are plugged. Any of these boards may be replaced without the need for soldering. Where a cable terminates on one board with solder joints, the other end of the same cable will have connectors. Visual examination of the assembly of these boards will reveal the procedures necessary for successful disassembly.

It is not so obvious how the Power Supply may be removed. Ten screws up from underneath the Chroma secure the supply. All ten (see Figure 3 - 4) should be removed from the bottom to detach the supply. The screws are threaded into standoffs holding the supply off the bed of the Chroma. The supply and rear panel are removed in one piece. When pulling the connectors from J1, J2 and J3, notice they are keyed identically and can be inadvertently connected incorrectly when re-installed. Refer to the Connection Diagram (Figure 3 - 5) and go by the colors of the wires.

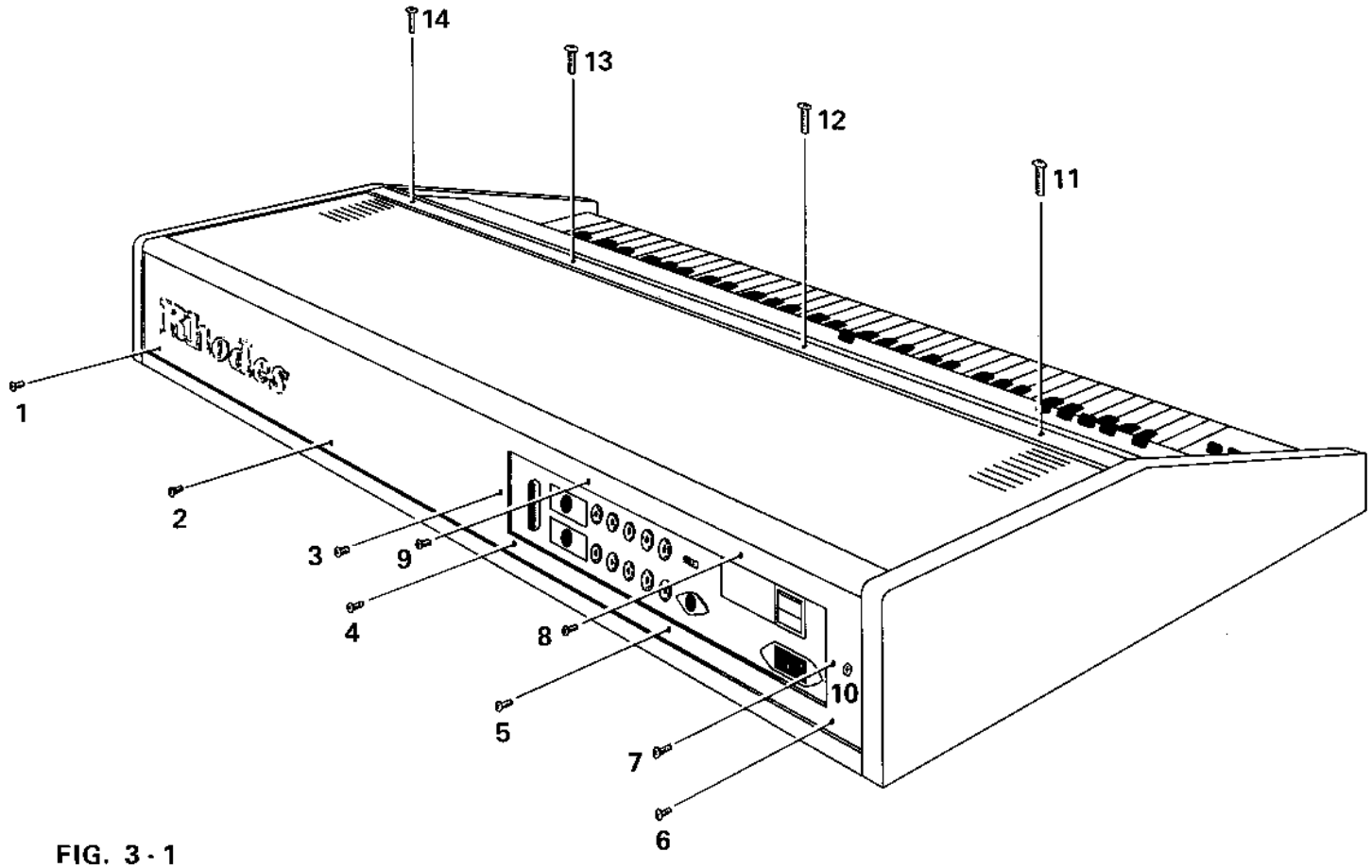


FIG. 3 - 1

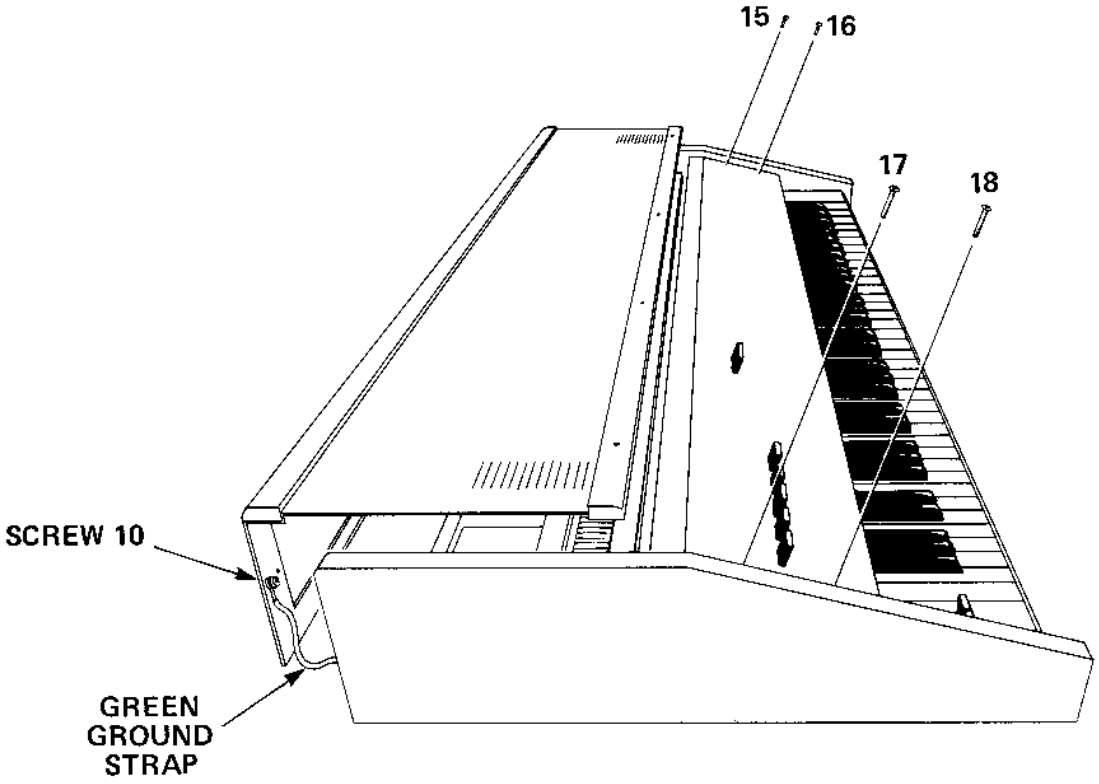

15
16
17
18
SCREW 10
GREEN
GROUND
STRAP

FIG. 3 - 2

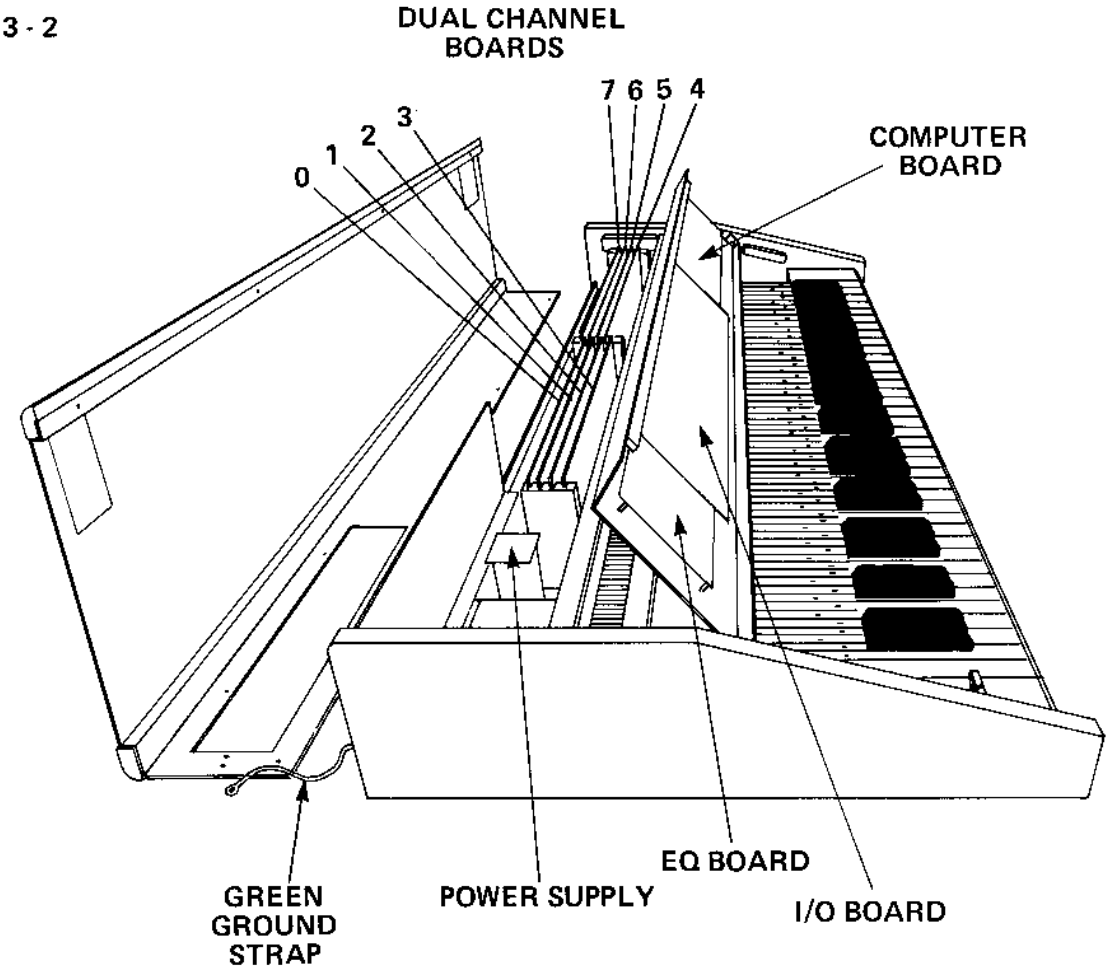

DUAL CHANNEL
BOARDS
7 6 5 4
3
2
1
0
COMPUTER
BOARD
EQ BOARD
GREEN
GROUND
STRAP
POWER SUPPLY
I/O BOARD

FIG. 3 - 3

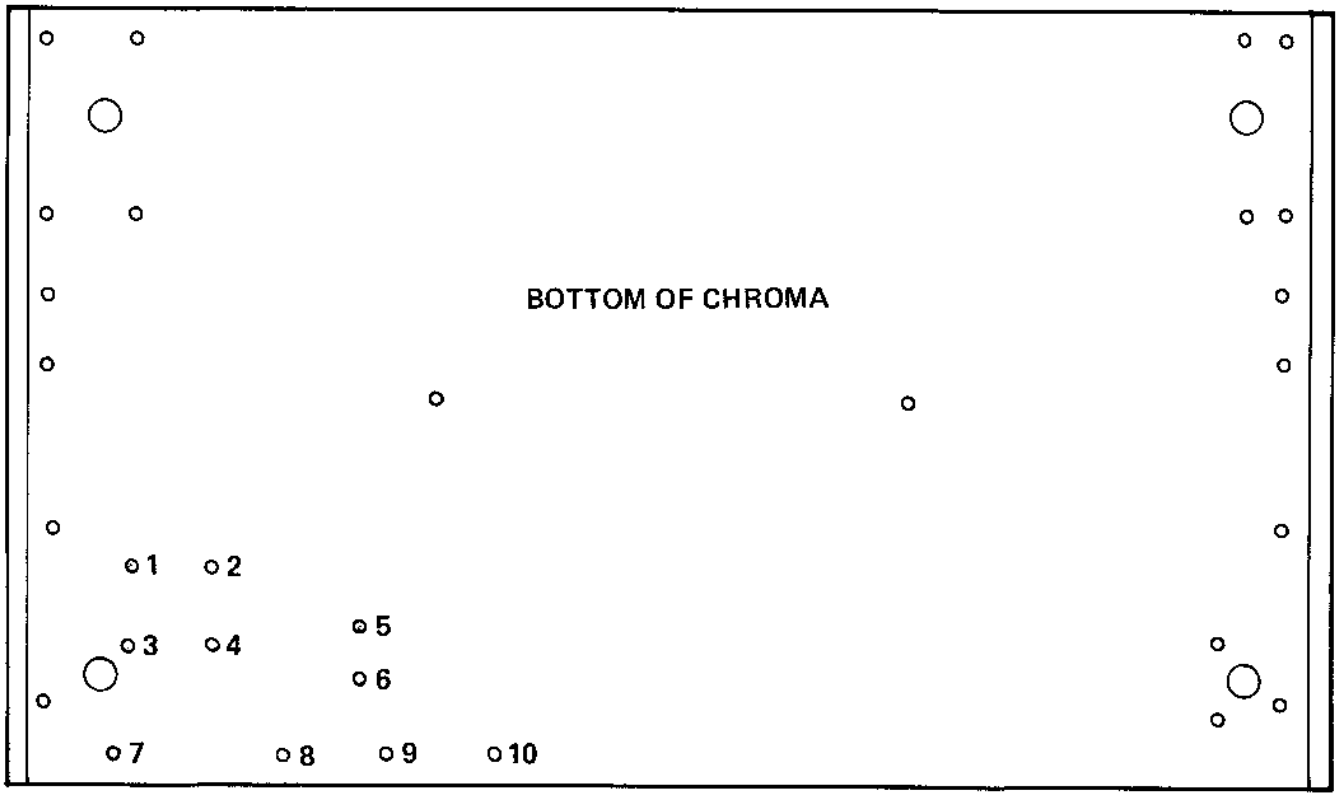


FIG. 3-4

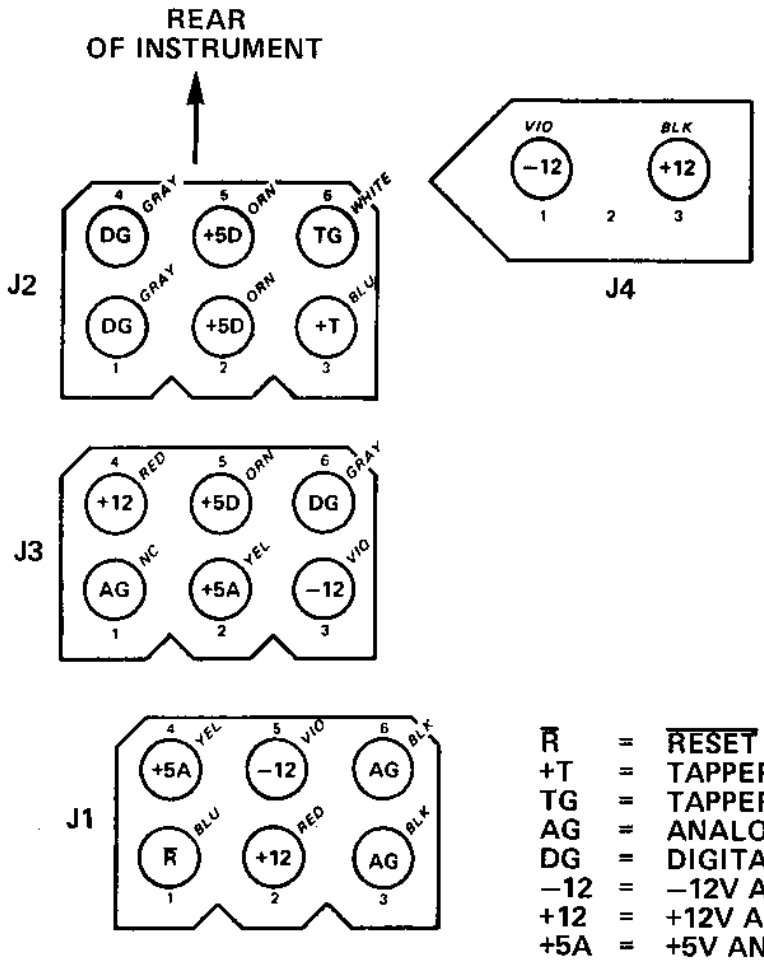


FIG. 3-5 CONNECTION DIAGRAM POWER SUPPLY

$\overline{R}$	=	$\overline{\text{RESET}}$
+T	=	TAPPER SUPPLY (+24V)
TG	=	TAPPER GROUND
AG	=	ANALOG GROUND
DG	=	DIGITAL GROUND
−12	=	−12V ANALOG SUPPLY
+12	=	+12V ANALOG SUPPLY
+5A	=	+5V ANALOG SUPPLY
+5D	=	+5V DIGITAL SUPPLY

During the auto tune routine, each of the 16 oscillators and filters are checked and tuned. This happens whenever the Chroma is turned on, when the [AUTO TUNE] switch is used or if a reset occurs. The eight Dual Channel Boards in the Chroma are labelled "0" through "7." (See Page 3 - 2 for board locations.) The computer will automatically turn off any Dual Channel Board that malfunctions and display an error message in the Data Readout. The message [ERR 6], for example, means that Dual Channel Board number "6" failed and has been turned off. Subsequently pressing [AUTO TUNE] will not affect the disabled board. The computer will ignore this Dual Channel until a reset or power-up occurs. The Chroma will operate normally, but with two less channels.

There are easily accessed hidden functions available by pressing [SET SPLIT] then a numbered switch on the right panel. While many of these are outlined in the owner's manual, certain ones are most useful in diagnosing problems. These are described in the following outline:

[SET SPLIT] [6] BATTERY TEST

Displays the non-volatile memory battery voltage in the Data Readout window. A typical reading displays [cell 3.16]. When the reading drops below 2.5 volts, the two "AA" size batteries on the Computer Board should be replaced.

[SET SPLIT] [7] DISABLE CHANNEL BOARD

This may be used to manually turn off a Dual Channel Board. If a channel board malfunctions, but was not automatically turned off during auto tune, it can be disabled manually. Play the keyboard until you hear the bad note, then while holding the key down (before playing another note) press [SET SPLIT] [7]. The channel board will turn off and be displayed as an error message in the Data Readout.

[SET SPLIT] [8] DISPLAY DISABLED BOARDS

If a channel board has been disabled, the Chroma will operate normally with two less channels. Selecting programs or editing will cause the Data Readout to display relevant data in place of the error message. To display the number of any disabled boards, use this function.

[SET SPLIT] [9] TAPPER ON/OFF

Alternately turns the Tapper off and on.

[SET SPLIT] [10] CASSETTE MODE

Selects automatic (motor sensing) or manual cassette mode. If the cassette will not load, this is the first thing to try — it may be in the wrong mode. The normal mode senses and controls the cassette motor, providing the polarity is such that the tip of the remote jack on the cassette recorder is positive in respect to the sleeve. The alternate mode allows use with cassettes that have no motor control, i.e. no remote jack.

[SET SPLIT] [26] MUTE A

Suppose you hear a bad note while playing up scale on the keyboard. Before turning it off with [SET SPLIT] [7], try muting all the "A" channels using [SET SPLIT] [26]. Now only the "B" channels will function. If a channel still outputs a bad note, it will, of course, be a "B" channel. Now you may hold down the bad note, turn it off with [SET SPLIT] [7] and read the board number in the Data Readout. You will have pinpointed the malfunction down to a single channel on a single board.

[SET SPLIT] [27] MUTE B

Turn off all "B" channels, similar to Mute A.

[SET SPLIT] [29] MUTE ALL

When using Mute A or Mute B, the "A" or "B" channels are silenced by turning off the "A"-VCA or the "B"-VCA through the sample and hold circuitry. "Mute All" differs in that the oscillators (both "A" and "B") are disconnected from the filters but the filters and amplifiers can still function. This lends itself to helping you differentiate between an oscillator and a filter problem. After determining a bad note is coming from a single channel on a single board you may use [SET SPLIT] [29] to mute all oscillators. A continuing bad sound suggests problems in the filters or more remotely in the amplifiers. No sound indicates the bad note was produced by the oscillator circuitry.

[SET SPLIT] [28] UNMUTE

Unmute channels. This unmutes [SET SPLIT] [26], [27], and [29].

[SET SPLIT] [30] TEST LEDS

Turns on all LEDs and display segments. This will provide maximum load to the Power Supply. Use this for checking a suspected marginal supply and for testing the LEDs. Select a program to restore normal operation.

[SET SPLIT] [31] SPECIAL RESET

It is possible to use some of the previously described functions to pinpoint an offending note only if the bad note plays. What if it was turned off automatically by the computer during an auto tune routine? No problem, use [SET SPLIT] [31] Special Reset. This will reset the main computer and call up an auto tune

routine but the computer is instructed to ignore any channels that malfunction. This will permit you to listen to all channels, even bad ones and to apply the previously described functions to help diagnose the problem. Additionally, this function orders an ascending channel assignment from board "0" to "7" with oscillator "B" first then oscillator "A." For example: if parameter "1" is set to value "0" (individual oscillators), the first note played will be channel board "0" oscillator "B," the second note will be channel board "0" oscillator "A" and so forth to the sixteenth note which will be channel board "7" oscillator "A." With parameter "1" set to value "1" (paired oscillators), the first note will be channel "0" both oscillators "B" and "A" and the eighth note channel "7" both oscillators "B" and "A."

[SET SPLIT] [50] RESET

This acts as a computer reset. It calls up an auto tune routine but differs from the [SET SPLIT] [31] Special Reset by ordering a descending channel assignment and the computer is not instructed to ignore malfunctions. The computer will automatically turn off malfunctioning boards. The descending channel assignment causes the first note to play oscillator "B" on board "7" the second note oscillator "A" on board "7" and the sixteenth note, oscillator "A" on board "0," providing you have selected the 16 channel mode with parameter "1" and no channels have been turned off automatically by the computer.

POWER DOWN/POWER UP

By turning off the Chroma and turning it on again, you will initiate a complete system reset. This calls up an auto tune routine, provides automatic fail/pass channel control to the computer but differs from previous resets by activating the power supply reset circuitry. The supply reset locks out the CMOS RAM (program memory) by deactivating the chip select lines until all supplies are in regulation. Further, the power down cycle deactivates these chip select lines prior to the supplies dropping out of regulation. Should you have problems relating to loss of program memory or overwriting garbage into program memory, be sure to check the power supply reset line during power down/power up.

In diagnosing Chroma problems, you will undoubtedly find a scope useful. Unfortunately, the strobe signals in the Chroma are fast pulses and may occur only once, depending on the system routine. The scope must be set up using a triggered sweep. An easy way to obtain correct sweep settings is to use the write tapper strobe on pin 7 of Z41, on the I/O Board. Sequentially, press a right panel membrane switch as you adjust the sweep, to capture the write tapper strobe. Each time you press the membrane switch, a write tapper strobe is generated. Once the sweep is set correctly, you can "look" for other strobes as dictated by the problem at hand. The I/O strobe decoder is a good place to start in most cases. If you are looking at the write timer mode line with a scope, you may see that this write strobe is repeated 2.5us apart. This was done to get around a ground noise problem that cropped up in some early units. Pretend there is only one strobe pulse for the point of view of analysis. Also, you may notice that the timer mode bits come out of latch Z42 with the middle bit inverted. This was a p.c. layout error that was easier to correct in the computer firmware. The computer thinks it is using modes 2, 3, 0, 1 and 6; but the three latch outputs will show modes 0, 1, 2, 3 and 4.

Listed below are values of supply current in two columns. The nominal current draw is measured under maximum load using [SET SPLIT] [30]. The other column lists the maximum current the supply will deliver before current limiting occurs. Calibration and checkout of the supply voltage levels are covered in Section 5.

SUPPLY	NOMINAL	MAXIMUM
+5V analog	125 milliamps	250 milliamps
+5V digital	2.3 amperes	2.5 amperes
+12V analog	500 milliamps	700 milliamps
-12V analog	500 milliamps	700 milliamps

SECTION 5. CALIBRATION AND CHECKOUT

All service centers are urged to obtain copies of the Chroma user manuals for performance, programming, sequencing and interfacing to have on hand as a reference source covering all aspects of operation.

A good starting point for calibration and checkout is the power supply. All three rectifier circuits are full-wave, but an open diode or trace may result in half-wave operation. The regulators will still work but filtering becomes less effective, increasing noise on the corresponding supply line output. This may cause erratic operation, intermittent glitches or tuning problems. For this reason, it is desirable to check ripple frequency whenever a Chroma is in for serrvice. Check the period of the ripple in all three circuits, on C3, C7 and C11. The period should be 8.3 millisec for 120Hz full-wave ripple. In addition, measure the amplitude of the preregulator ripple. This should never exceed 0.5Vp-p. If higher than 0.5Vp-p tighten the mounting screws on C3 that hold the overvoltage protector. It is good practice to mount the wire terminals beneath the Overvoltage Protector Board for maximum conductivity. These connections are critical.

The preregulator DC voltage on C3 (in reference to ground) should be adjusted so the minimum dip in the ripple waveform is at a DC level of 6.2 volts. The peak should be about 6.6 volts. Minimum dip should not drop below 6.0VDC. Maximum peak should not rise above 7.0VDC. The adjustment is made by changing the bias on transistor Q3. Two versions of the printed circuit fabrication exist for this supply. In one version a potentiometer (R46) is provided to correctly bias Q3. Simply adjust R46 for ripple dip of 6.2VDC on C3. In the other version, resistor R3 must be changed in value (usually by shunting it) to set the dip to 6.2 VDC. We suggest using a decade box first, then soldering in the correct value. Use a DC scope to check the DC level of the dip and peak, a DVM will not suffice. Preregulator voltage that is two low will cause erratic operation.

The +5V analog supply provides the reference voltage for the D/A converters. Calculations indicate that the auto-tune functions operate closer to center range when the +5V analog supply is adjusted slightly on the high side. Empirical data from the field reinforces this condition. Set the +5V analog supply to +5.05VDC by adjusting potentiometer R22. Use a DVM to measure from the yellow wire at J1-4 on the supply to chassis ground. This supply voltage if set two low will adversely affect tuning and may cause the computer to fail Dual Channel Boards.

Although no adjustments are necessary for the +12V or -12V analog, check them anyway to ensure they are within 5% of their nominal voltage. The +5V digital should not dip below 4.9V and will usually be slightly high after setting the +5V analog to +5.05, as this is where it takes its reference.

The next circuit needing calibration is on the I/O Board. The output buffer in the DAC circuit is a FET-input op-amp with an offset null trimmer. The offset voltage must be set to within 100uv of zero. Connect a DVM (3½ or 4 digit) between test point 0 and test point 1 on the I/O Board. Adjust potentiometer R1 for ±.0001VDC. This calibration must be correct to prevent tuning problems.

Prior to further calibration and checkout, it is necessary to set up a "scratch" patch. Activate both [EDIT A] and [EDIT B] functions, then while pressing and holding the [PARAM SELECT] switch, press each of the 50 numbered switches on the right panel. This disables all pitch and pulse width modulation. All parameters will now be set to their default "scratch" setting. Be sure the [NO LINK] LED is on and that all transpose LEDs are off. Playing a key using this unmodified "scratch" patch results in a raw sawtooth wave sound. The "scratch" patch will not affect any of the 50 programs stored in memory unless you use the [STORE] switch.

You may now check and calibrate the Dual Channel Boards following one of the procedures outlined below:

TRIM PROCEDURE: They only adjustment in the synthesizer circuit is the charge pump current, which is adjusted by R1 (R2). This adjustment affects the voltage level at the bottom of the sawtooth swing (the top is fixed at 5 volts). This in turn affects the pulse width, which suggests an easy way to do the trim. After setting up the "scratch" patch, modify parameter 3 (keyboard alg) to value 3 (all channel poly), this gives a common control voltage value to all 16 oscillators for ease of calibration. Set wave shape parameter (No. 33) to value 1 (pulse), and set pulse width parameter (No. 34) to 32 (50% duty cycle).

Connect your scope to TP1 on any channel board, set it for negative edge triggering, and adjust for a stable display. It is important that you trigger off the falling edge of the pulse that you see. Fine-adjust the horizontal sweep rate until the low portion of the oscillator pulse cycle lasts from exactly the first graticule division on the scope to the middle division. If you are looking at a perfect square wave, obviously the next falling edge of the cycle will appear perfectly lined up with the rightmost division on the scope face. Turning the trimmer R1 will not affect the low portion of the cycle, but will only shorten or lenghten the the high portion of the cycle. Adjust this until you see the second falling edge perfectly lined up with the last graticule division. Repeating this test for each channel simply involves moving the probe to the next test point, readjusting the horizontal sweep speed so that the low part of the cycle takes exactly half the screen, and adjusting the trim so that the entire cycle takes up the full screen.

ALTERNATE TRIM PROCEDURE: The pulse width can be trimmed well enough without a scope by ear. This takes a bit longer, as one has to get the correct oscillator to sound before doing each adjustment. The easiest way to do this, is to set up a simple sound (one without pitch or pulse width modulation) using Patch 0, so that each note is played by a single oscillator. If the Wave Shape parameter (No. 33) is set to 0 and the Width parameter (No. 34) is set to 32, the fundamental frequency of each note should be suppressed, causing the notes to sound an octave higher. To understand this better, try varying the Width parameter on either side of setting 32. If an oscillator is incorrectly trimmed, the fundamental frequency will be nulled out at some setting other than 32. Once you have established that you are adjusting the oscillator you are listening to, you can easily perform the trim. Don't be thrown by the fact that the pitch is varied too. Just adjust to null out the fundamental. When you are through, you can do an auto-tune.

The easiest way to determine which channel you are playing is to reset the instrument (press [SET SPLIT] [50]). If you subsequently play sixteen different notes (a chromatic scale, for instance), the channels will always be heard in reverse order, starting with the B oscillator (R2 trim) on board 7. Board 7 is the board closest to the right rear corner of the instrument. The boards are ordered in a U-shaped sequence, so that board 0 is the board closest to the audio outputs. If you bump an extra note during this procedure, or get otherwise confused, just press [SET SPLIT] [50] again to reorder the channel assignment.

Once the Dual Channels have been "trimmed" you may want to check tuning. Use the "scratch" patch but change patch parameter [1] from value "0"to value "1." Instead of one oscillator per note the Chroma will assign two per note. Tuning is checked by listening to the oscillators beat together. Proceed by resetting the Chroma pressing [SET SPLIT] [31]. Play the "C" one ocatve above middle "C" and count the beats over a 10 second period then divide by 10 to determine actual beats for one second. Repeat this going up-scale until eight notes have been played. Anything over two beats per second is unacceptable. An offending Dual Channel Board may be shut off by pressing [SET SPLIT] [7], (see the Diagnostic Chart). The data readout in the little display window will show an error followed by the board number that was shut off. Of course more than one board may be shut off using this feature. Example: The display [ERR 05] means that board "0" and board "5" are shut off.

If you find an unacceptable Dual Channel Board, swapping positions may help in analyzing the problem. Suppose the tuning is out of specification on the third note you play. Activating [SET SPLIT] [7] causes [ERR 2] to be displayed. Swap board "2" with board "1" (with power shut off) then try again. If the out of tune condition moves to position "1" [ERR 1] the problem is on that Dual Channel Board. If the out of tune condition still indicates [ERR 2], the problem is not on the Dual Channel, but likely in the strobing circuits on the Channel Mother Board. Random out of tune conditions are likely to be in the DAC circuits on the I/O Board, or problems in the +5V analog supply.

An alternate method to check tuning follows: Use the "scratch" patch but set Wave Shape parameter (No. 33) to value "1" and Width parameter (No. 34) to value "32." Press [SET SPLIT] [31] to auto-tune and order the channels. Using a tuning strobe or meter check each of the 16 oscillators starting with middle "C" and play chromatically up-scale. Do not stop at one octave, continue until 16 different notes have been played. Measure each note individually for number of hundreds of semitones off center frequency. Each note should be within 2.5 cents of its center frequency.

The remaining adjustments have to do with keyboard action. Refer to Figure 5 - 1. Measure the depth of keydown on a low, middle and high note. The depth should be 3/8 inch from keytop to keytop at the front edge of the key. Less than 3/8 inch key travel means the Damper Bar is too low. Figure 5 - 2 illustrates the hardware securing the Damper Bar. Loosen screws 1 and 2 and nuts 3, 4, 5 and 6. The Damper Bar should be positioned so that the lead weight just touches the felt with normal full keydown pressure. Check this on both ends and near the two center brackets (some early Chroma's have only one center bracket). After tightening all mounting hardware, check Damper Bar height. Press a key down with one hand and with the other hand grasp the wood key shank just forward of the lead weight. Pull against the Damper Bar felt. Proper adjustment results in restraint of further movement. If the Damper Bar is too high, the lead weighted end of the key will pull up higher against the felt even though you are holding the key full down with your other hand. As mentioned previously, adjusting the Damper Bar too low will restrict the keydown movement to less than 3/8 inch.

The left and right stack switch boards are mounted with three (3) screws going through elongated holes into "T" nuts (see Figure 5 - 3). Loosening these screws allows the stack switches to be moved up or down to their correct position. Set the stack switch boards so that the top (normally open) leaf travels upward about 1/32" after closing (as shown in Figure 5 - 4) before the key stops.

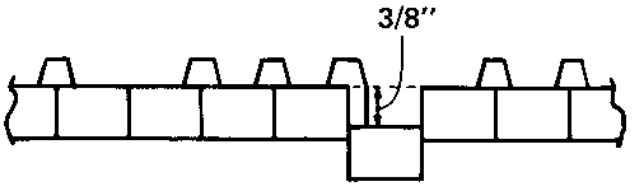


FIG. 5 - 1 KEY DEPTH MEASUREMENT

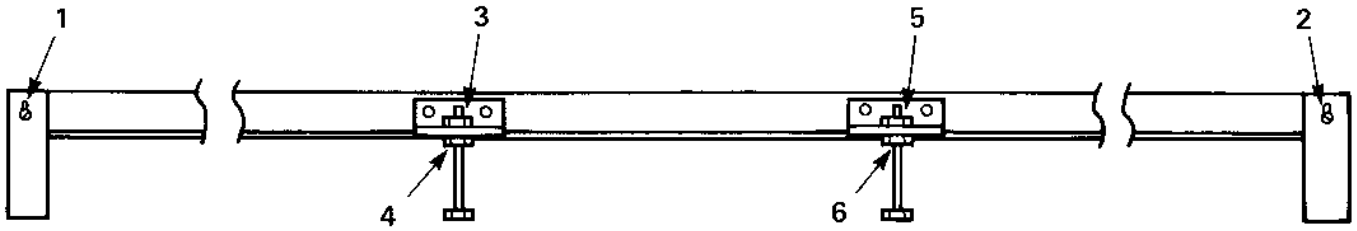


FIG. 5 - 2 DAMPER BAR ASSEMBLY

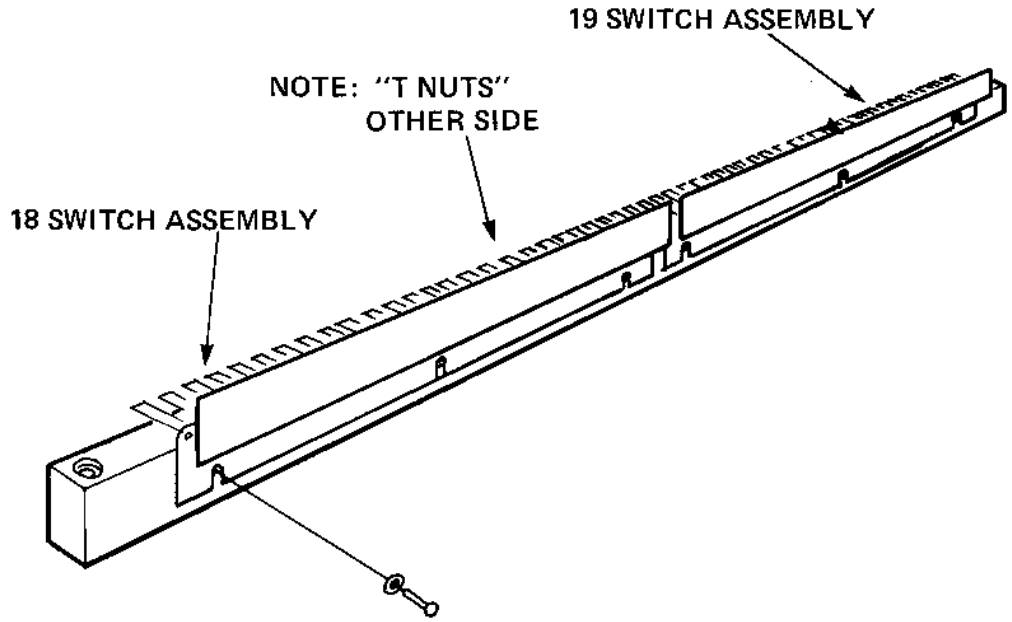


FIG. 5 - 3 STACK SWITCH ASSEMBLIES

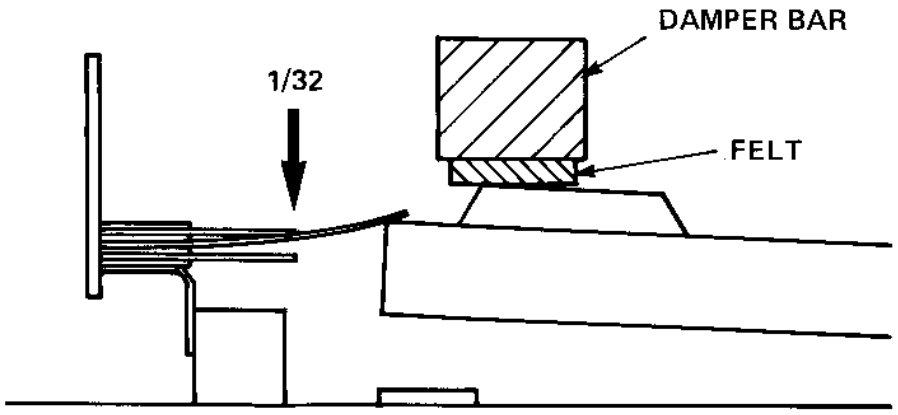
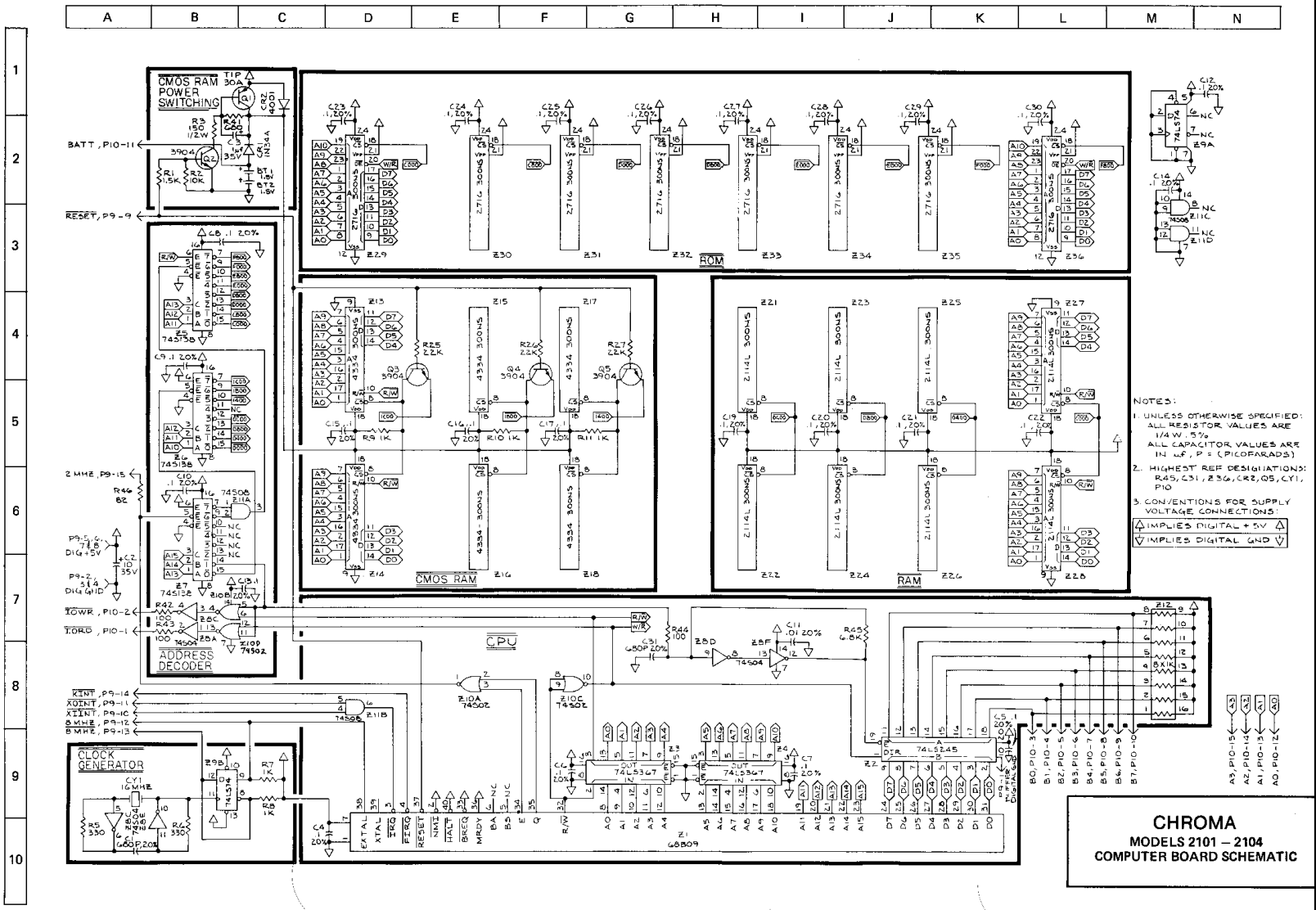


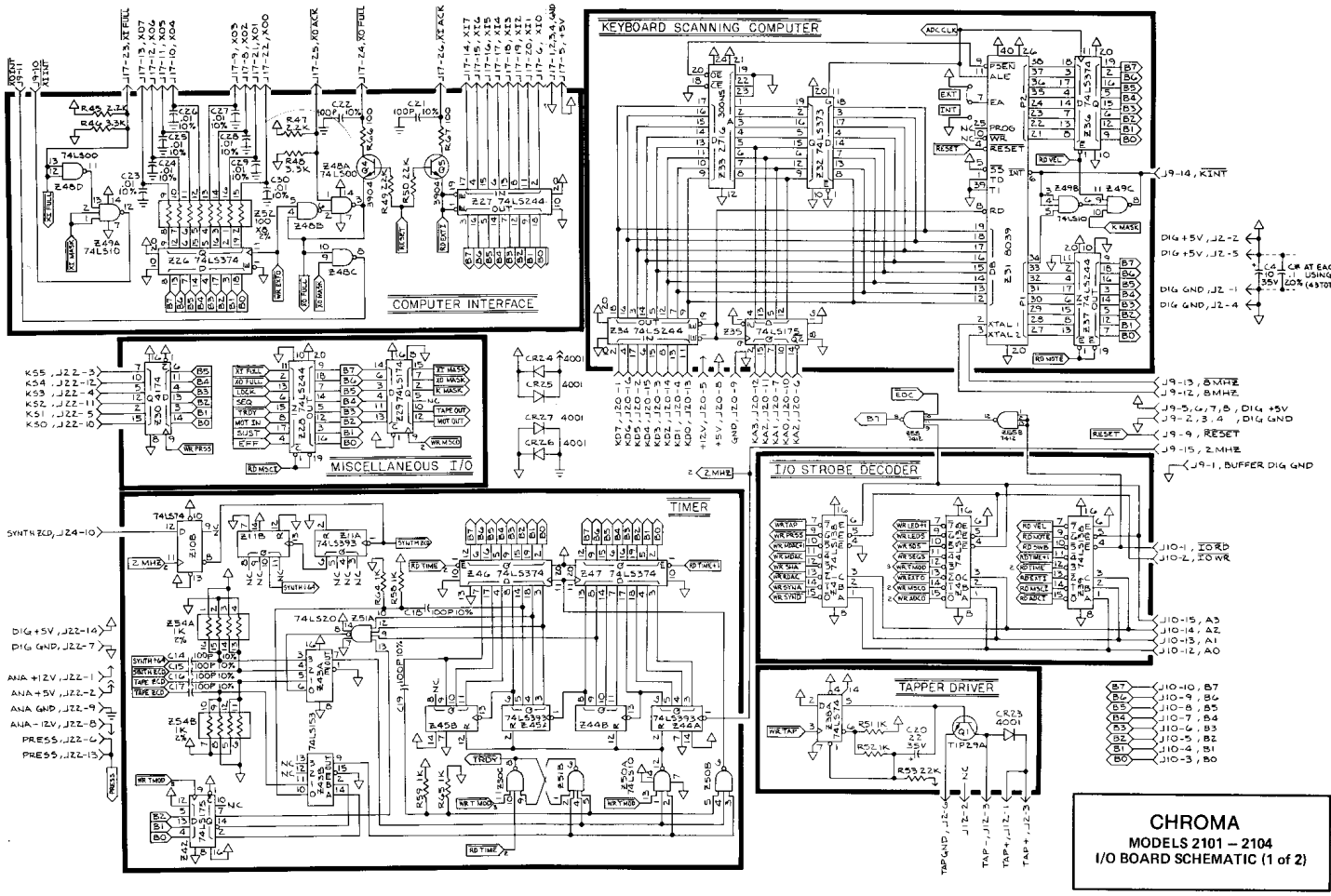
FIG. 5 - 4

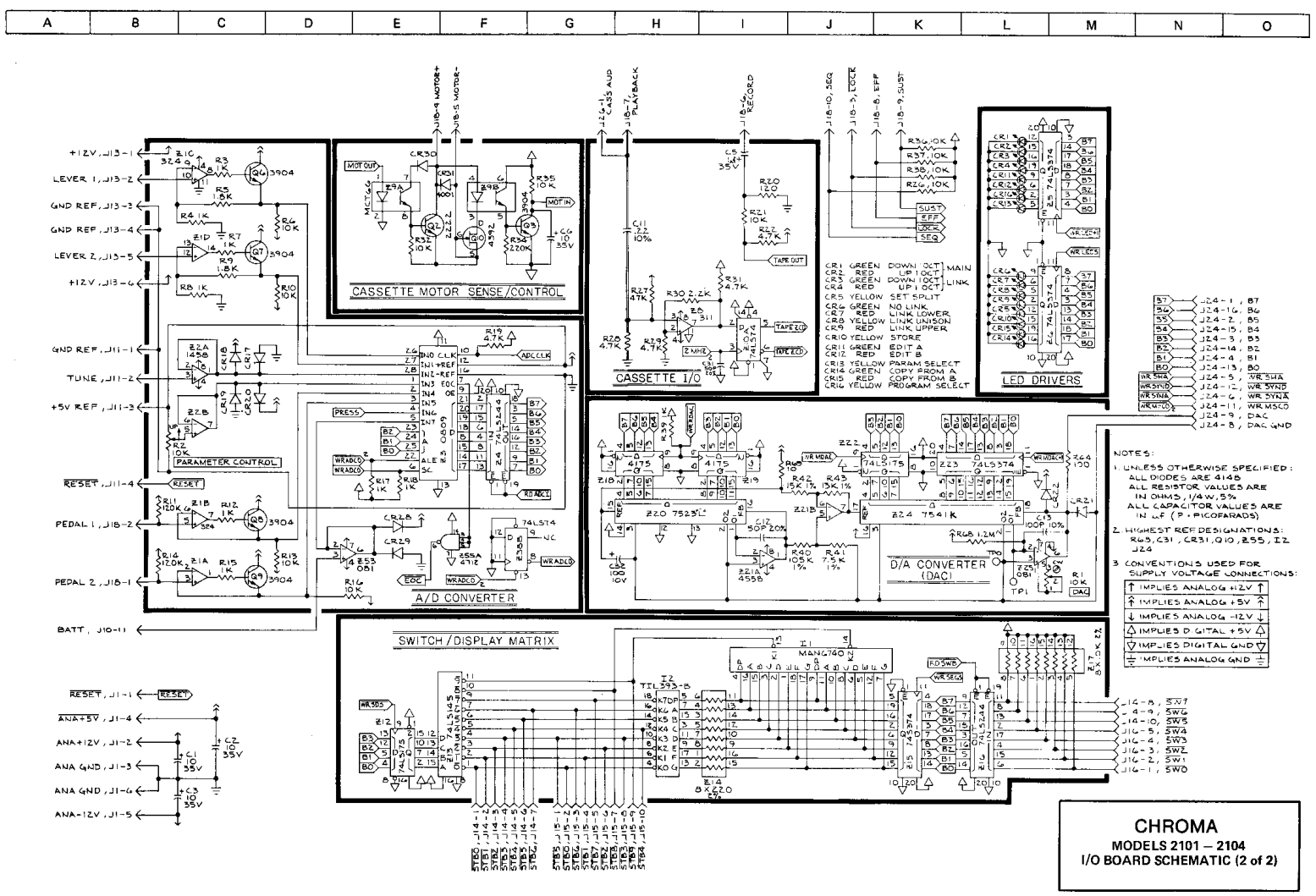


CHROMA

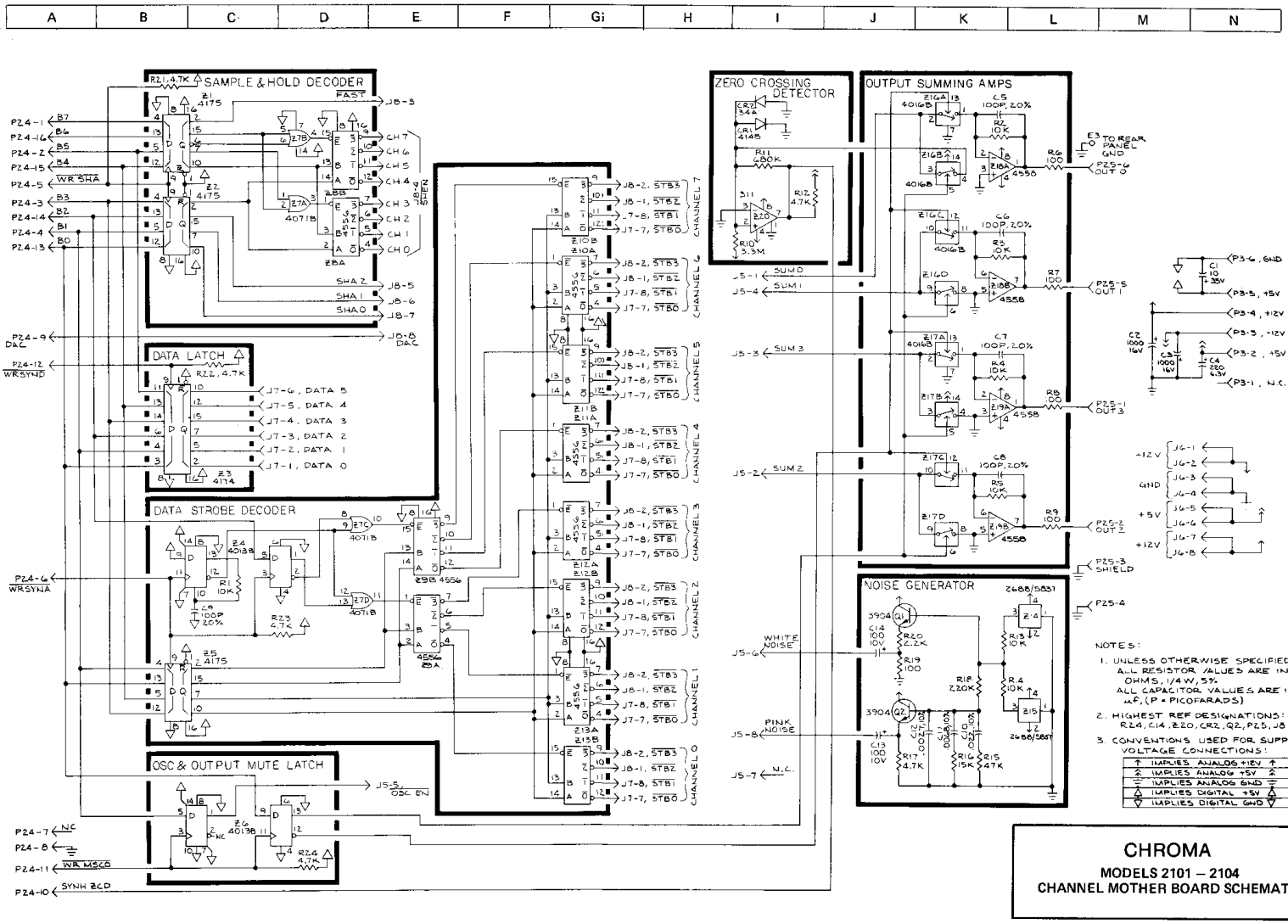
MODELS 2101 – 2104

COMPUTER BOARD SCHEMATIC


KEYBOARD SCANNING COMPUTER
COMPUTER INTERFACE
MISCELLANEOUS I/O
TIMER
I/O STROBE DECODER
TAPPER DRIVER
CHROMA
MODELS 2101 – 2104
I/O BOARD SCHEMATIC (1 of 2)

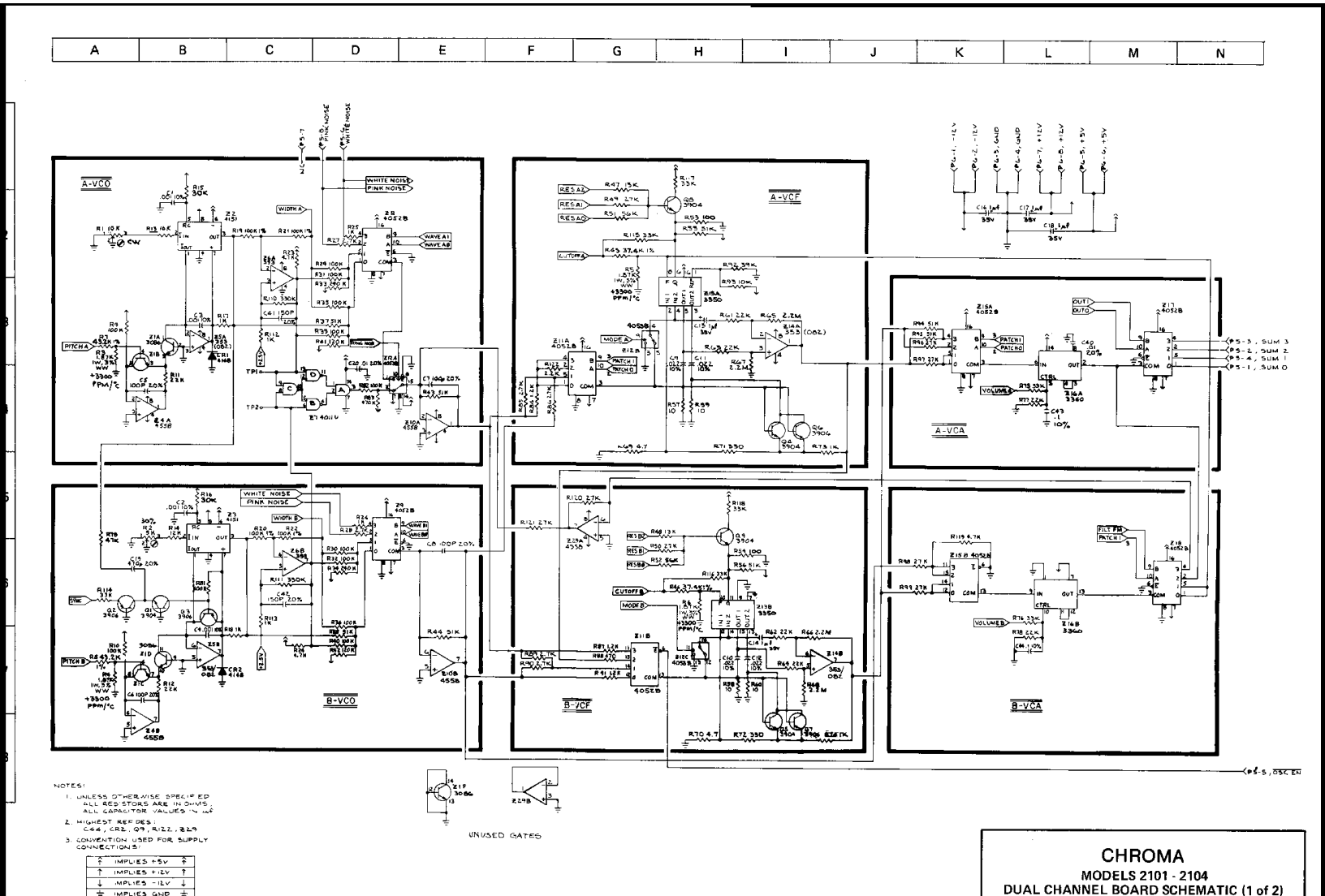


CHROMA
MODELS 2101 – 2104
I/O BOARD SCHEMATIC (2 of 2)



CHROMA

MODELS 2101 – 2104
CHANNEL MOTHER BOARD SCHEMATIC



NOTES:

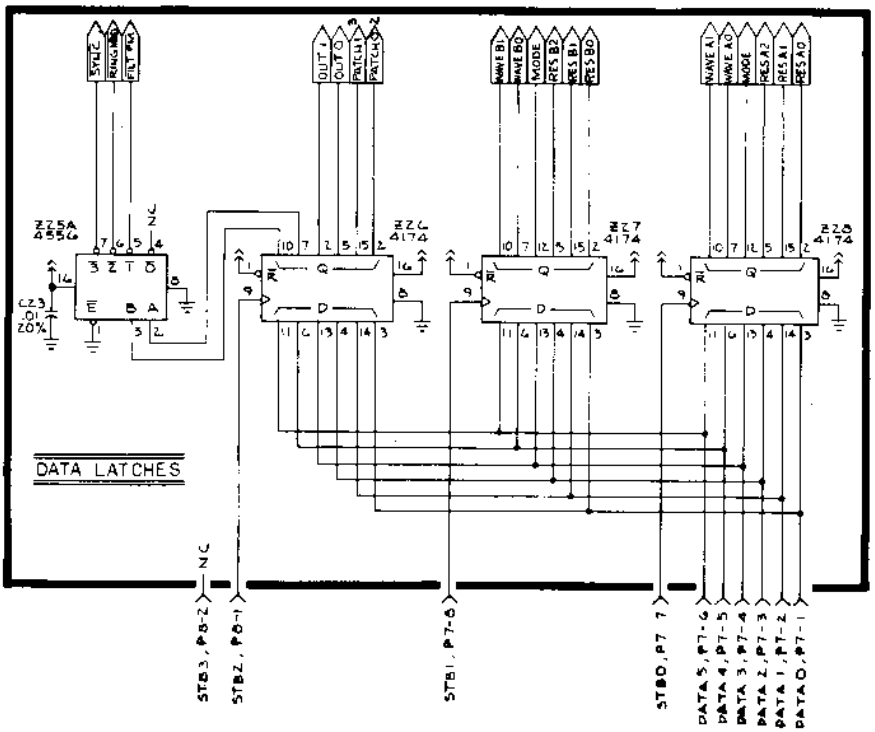
1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS, ALL CAPACITOR VALUES IN μF
2. HIGHEST REFDES: C44, CR2, Q9, R122, Z29
3. CONVENTION USED FOR SUPPLY CONNECTIONS:

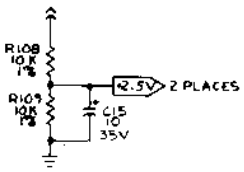
↑	IMPLIES +5V
↑	IMPLIES +12V
↓	IMPLIES -12V
⏚	IMPLIES GND

CHROMA

MODELS 2101 - 2104

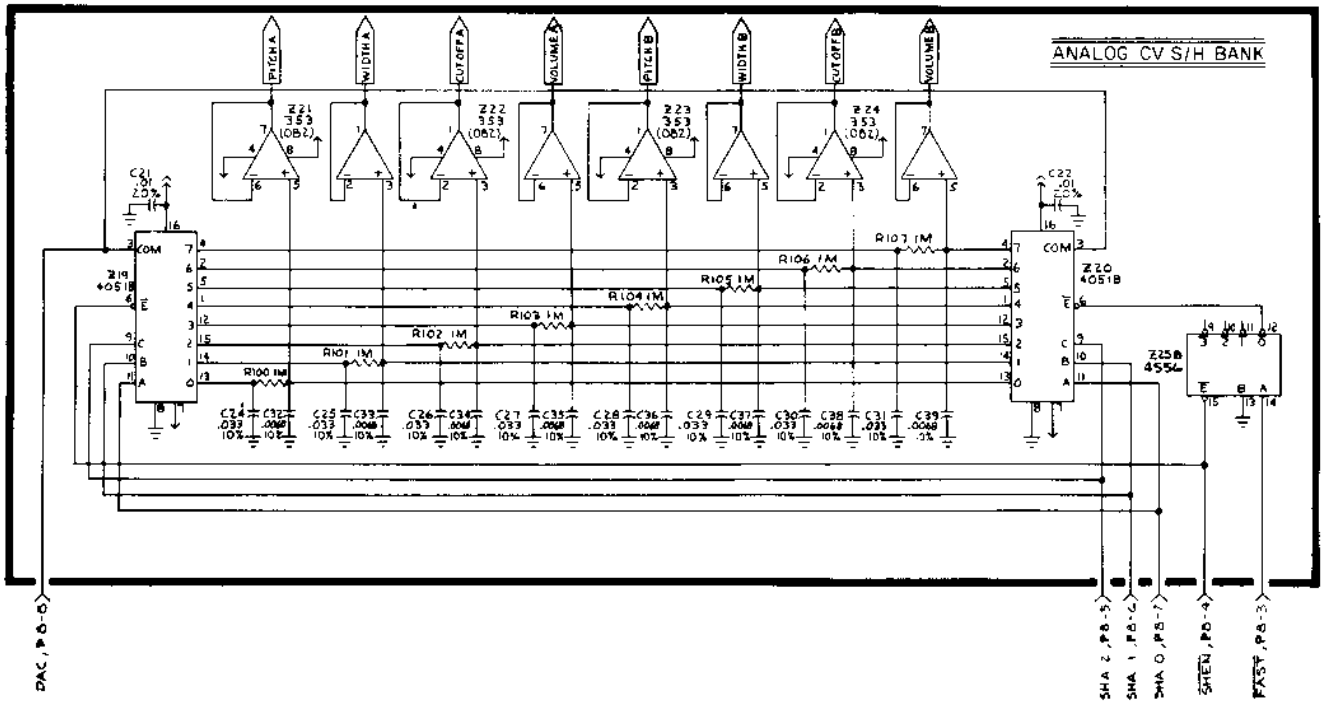
DUAL CHANNEL BOARD SCHEMATIC (1 of 2)

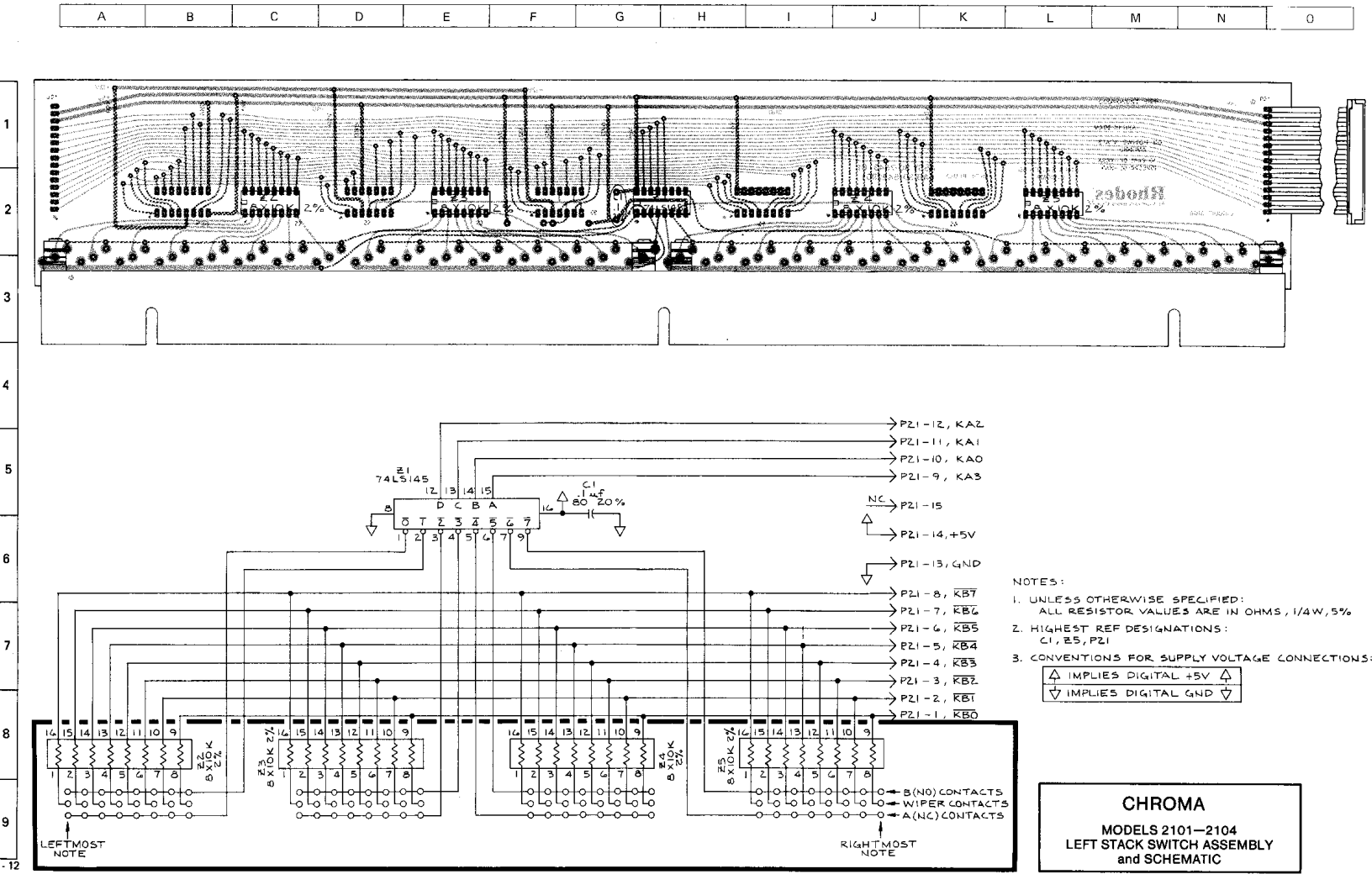




CHROMA

MODELS 2101 - 2104
DUAL CHANNEL BOARD ASSEMBLY and DUAL CHANNEL BOARD SCHEMATIC (2 of 2)



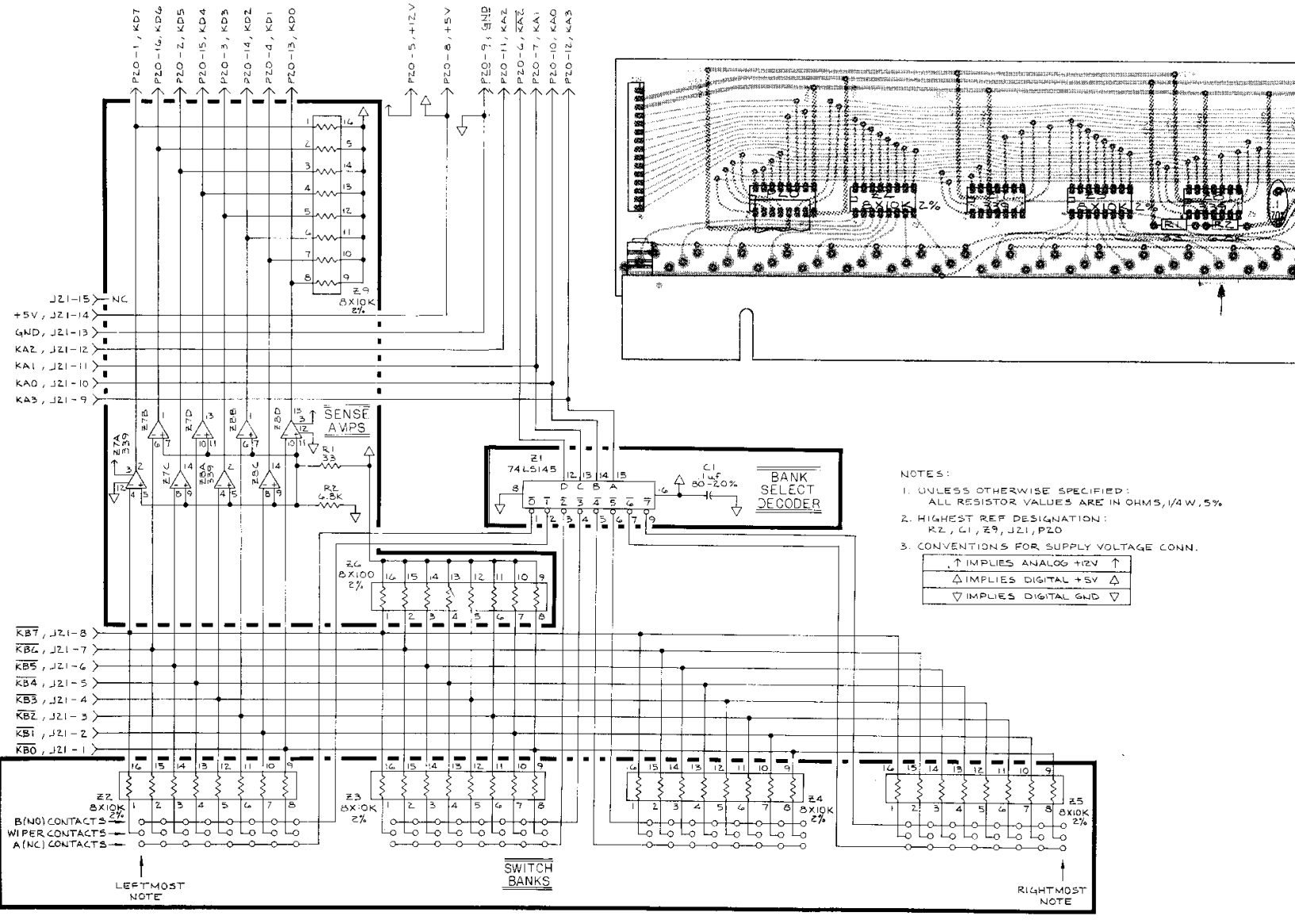


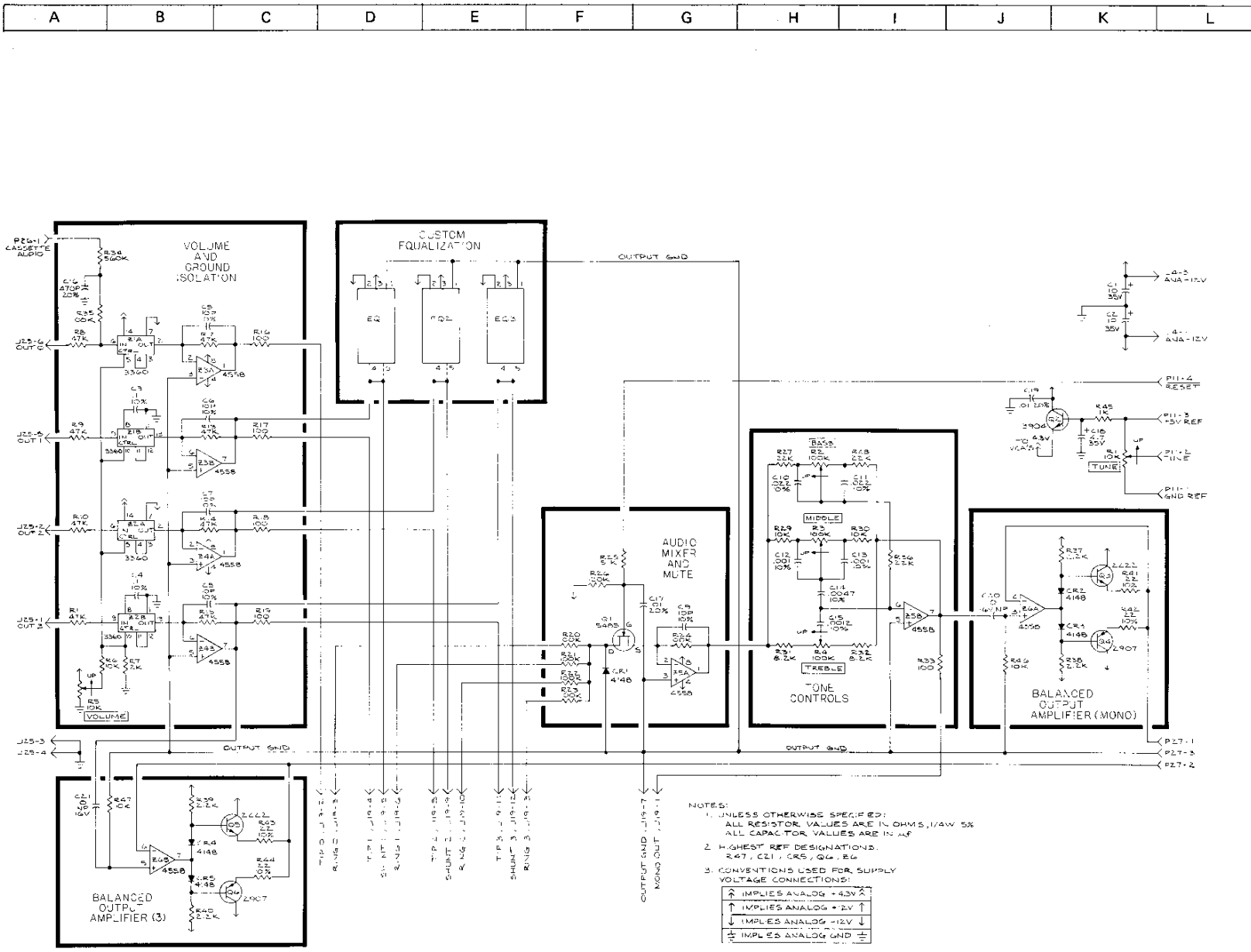
NOTES:

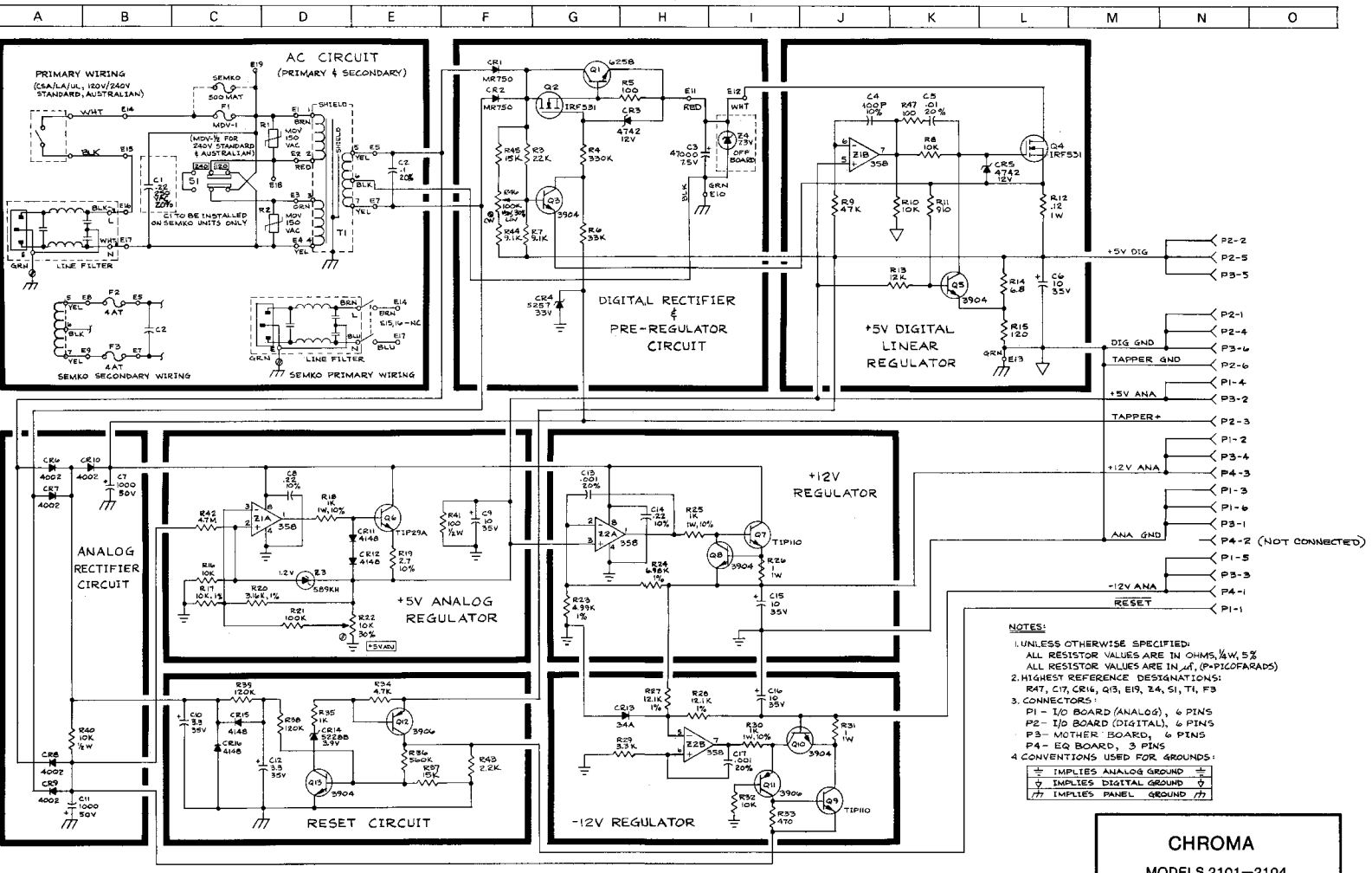
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%
2. HIGHEST REF DESIGNATIONS:
   C1, Z5, P21
3. CONVENTIONS FOR SUPPLY VOLTAGE CONNECTIONS:
   △ IMPLIES DIGITAL +5V △
   ▽ IMPLIES DIGITAL GND ▽

CHROMA

MODELS 2101—2104
LEFT STACK SWITCH ASSEMBLY and SCHEMATIC


A
B
C
D
E
F
G
H
I
J
K
L
M
PZ0-1, KD7
PZ0-16, KD6
PZ0-2, KD5
PZ0-15, KD4
PZ0-3, KD3
PZ0-14, KD2
PZ0-4, KD1
PZ0-13, KD0
PZ0-5, +12V
PZ0-8, +5V
PZ0-9, GND
PZ0-11, KA2
PZ0-6, KA2
PZ0-7, KA1
PZ0-10, KA0
PZ0-12, KA3
Z9 8X10K 2%
J21-15 NC
+5V, J21-14
GND, J21-13
KA2, J21-12
KA1, J21-11
KA0, J21-10
KA3, J21-9
SENSE AMPS
Z7A 339
Z7B
Z7C
Z7D
Z8A 339
Z8B
Z8C
Z8D
R1 33
R2 6.8K
Z1 74LS145
BANK SELECT DECODER
C1 1uF 80-20%
Z6 8X100 2%
KB7, J21-8
KB6, J21-7
KB5, J21-6
KB4, J21-5
KB3, J21-4
KB2, J21-3
KB1, J21-2
KB0, J21-1
Z2 8X10K 2%
Z3 8X10K 2%
Z4 8X10K 2%
Z5 8X10K 2%
B(NO) CONTACTS
WIPER CONTACTS
A(NC) CONTACTS
LEFTMOST NOTE
SWITCH BANKS
RIGHTMOST NOTE
NOTES:
1. UNLESS OTHERWISE SPECIFIED: ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%
2. HIGHEST REF DESIGNATION: R2, C1, Z9, J21, PZ0
3. CONVENTIONS FOR SUPPLY VOLTAGE CONN.
↑ IMPLIES ANALOG +12V ↑
△ IMPLIES DIGITAL +5V △
▽ IMPLIES DIGITAL GND ▽


A
B
C
D
E
F
G
H
I
J
K
L
VOLUME AND GROUND ISOLATION
CUSTOM EQUALIZATION
AUDIO MIXER AND MUTE
TONE CONTROLS
BALANCED OUTPUT AMPLIFIER (MONO)
BALANCED OUTPUT AMPLIFIER (3)
OUTPUT GND
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTOR VALUES ARE IN OHMS, 1/4W 5%
ALL CAPACITOR VALUES ARE IN uF
2. HIGHEST REF DESIGNATIONS.
R47, C21, CR5, Q6, B6
3. CONVENTIONS USED FOR SUPPLY VOLTAGE CONNECTIONS:
↑ IMPLIES ANALOG +4.3V ↑
↑ IMPLIES ANALOG +12V ↑
↓ IMPLIES ANALOG -12V ↓
⏚ IMPLIES ANALOG GND ⏚



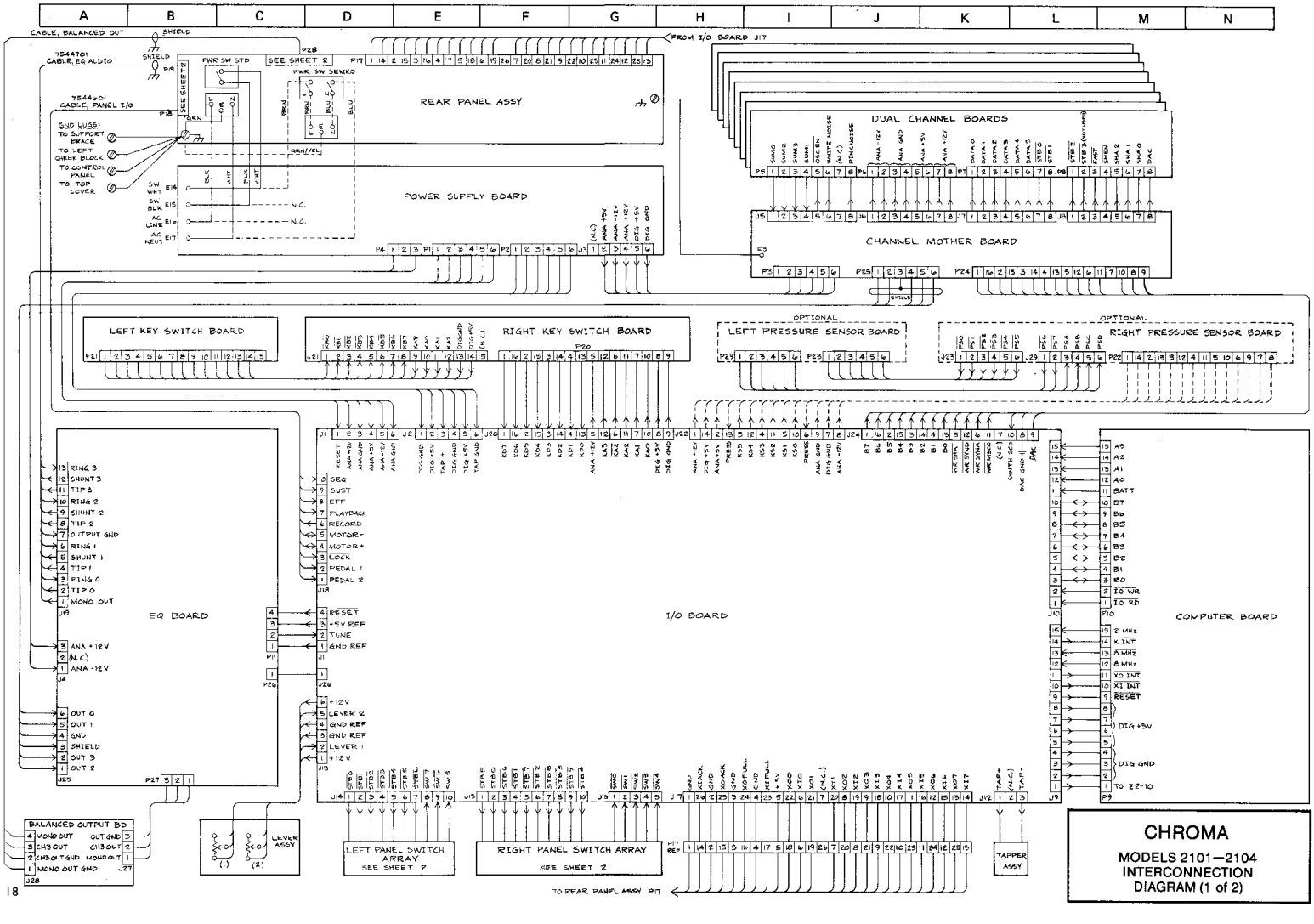
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTOR VALUES ARE IN OHMS, ¼W, 5%
   ALL RESISTOR VALUES ARE IN μf, (P=PICOFARADS)
2. HIGHEST REFERENCE DESIGNATIONS:
   R47, C17, CR16, Q13, E19, Z4, S1, T1, F3
3. CONNECTORS:
   P1 – I/O BOARD (ANALOG), 6 PINS
   P2 – I/O BOARD (DIGITAL), 6 PINS
   P3 – MOTHER BOARD, 6 PINS
   P4 – EQ BOARD, 3 PINS
4. CONVENTIONS USED FOR GROUNDS:

⏚	IMPLIES ANALOG GROUND
▽	IMPLIES DIGITAL GROUND
⏚	IMPLIES PANEL GROUND

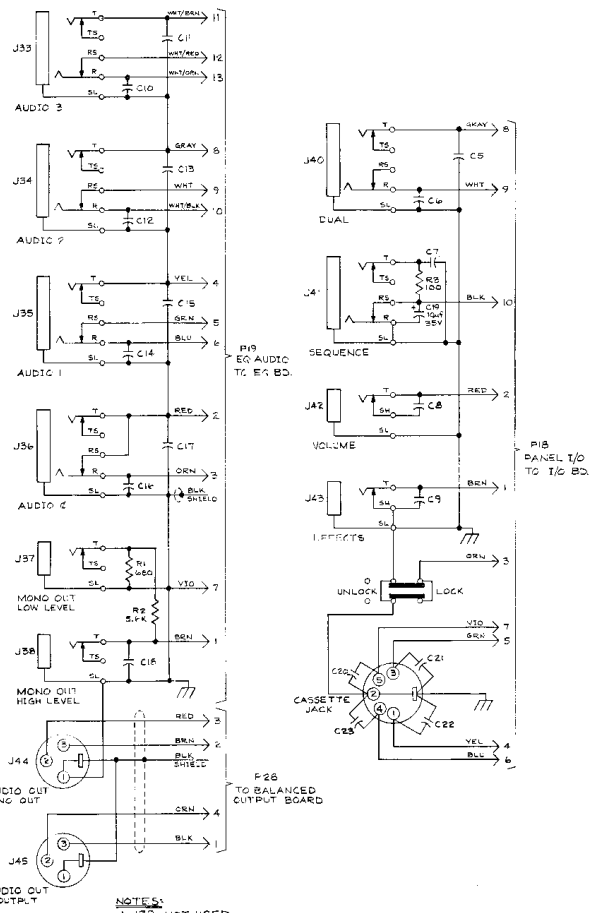
CHROMA

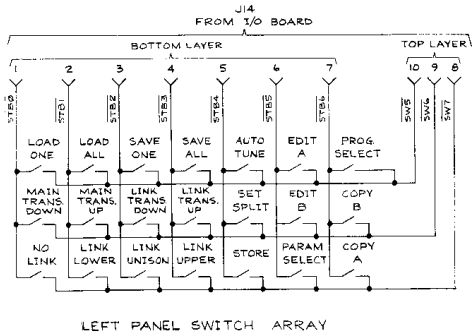
MODELS 2101—2104
POWER SUPPLY SCHEMATIC



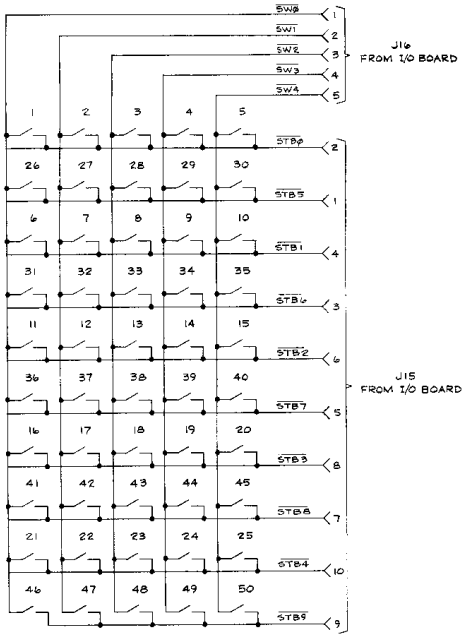
CHROMA

MODELS 2101—2104 INTERCONNECTION DIAGRAM (1 of 2)





LEFT PANEL SWITCH ARRAY

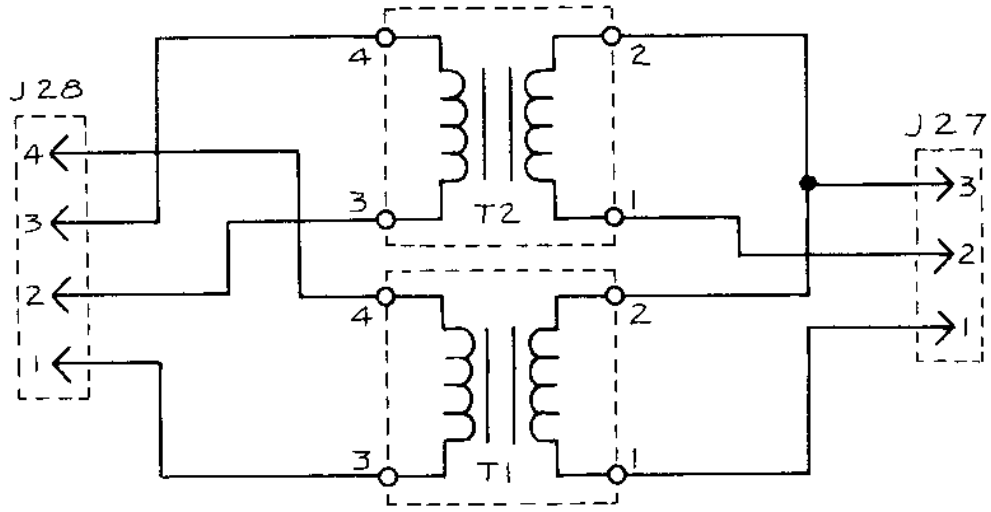


RIGHT PANEL SWITCH ARRAY

NOTES:
1. U39 NOT USED
2. UNLESS OTHERWISE SPECIFIED:
ALL RESISTOR VALUES ARE IN OHMS, ¼W 5%
ALL CAPACITOR VALUES ARE 100 PICOFARADS, 50V, 10%

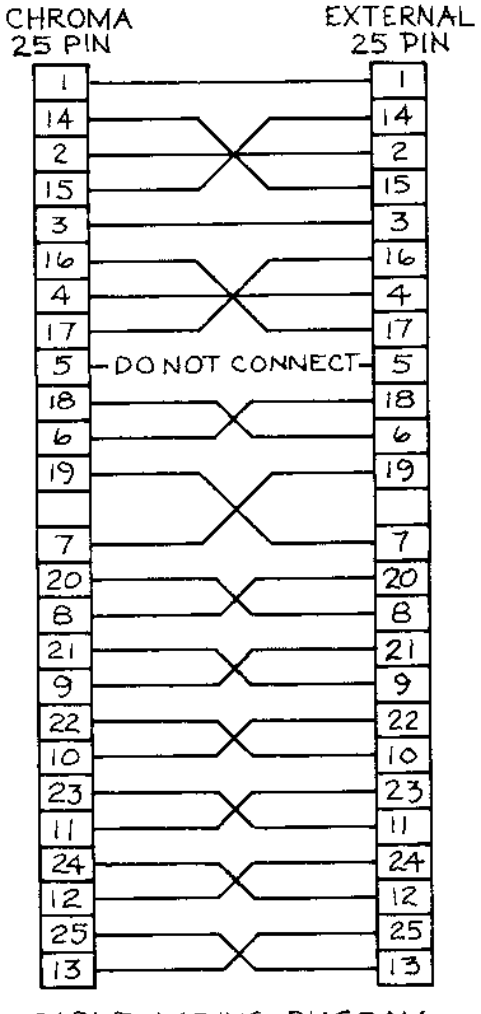
CHROMA

MODELS 2101—2104
INTERCONNECTION
DIAGRAM (2 of 2)



CHROMA

MODELS 2101—2104
BALANCED OUTPUT SCHEMATIC



CABLE WIRING DIAGRAM

CHROMA

MODELS 2101—2104
INTERFACE CABLE SCHEMATIC

COMPUTER BOARD, 30-7225301

REFERENCE	CHROMA PART NO.	MFG. NO.	DESCRIPTION
C2	30-1103005	------	CAP ELECT 10UF 35V 50-10
C3	30-1103201	------	CAP ELECT 1UF 35V 20%
CR1	30-1200101	1N34A	DIODE GE
CR2	30-1200201	4001	RECT 50V 1A
Q2,3,4,5	30-1302901	3904	TSTR NPN GP
Q1	30-1305001	TIP30A	TSTR NPN POWER
Z10	30-1401803	74S02	IC GATE 4X2I
Z11	30-1403403	74S08	IC GATE 4X2I, AND
Z8	30-1406602	74S04	IC HEX INVERT
Z9	30-1406701	74LS74	IC DUAL D FF PRST CLEAR
Z1	30-1412101	68B09	IC MICRO COMPUTER
Z21-28	30-1412601	2114L	IC RAM 1K X 4 NMOS
Z2	30-1412701	74LS245	IC DRIVER BI-DIRECT OCT
Z5,6,7	30-1413101	74S138	IC 1 OF 8 DEC
Z3,4	30-1413501	74LS367	IC HEX BUFFER 3 ST
Z13-18	30-1414001	6514-9, 65114-30,4334P-3	IC RAM 1K X 4 CMOS 300NS
Z12	30-1414104	------	IC RES NETWORK 1K 16 PIN ¼W 2%
For Z29-36	30-2102705	------	SOCKET DUAL IN LINE 24 PIN LP
For Z1	30-2102706	------	SOCKET DUAL IN LINE 40 PIN LP
For Z13-18, Z21-28	30-2102707	------	SOCKET DUAL IN LINE 18 PIN LP
For P9,10	30-2107701	------	CONN HOUSING FLAT FLEX 15 PIN
P9,10	30-2204701	------	CABLE FLAT FLEX 15 COND 15"
CY1	30-2600302	------	CRYSTAL 16MHZ
Z29	30-5603201	------	IC EPROM PROGRAMMED
Z30	30-5603202	------	IC EPROM PROGRAMMED
Z31	30-5603203	------	IC EPROM PROGRAMMED
Z32	30-5603204	------	IC EPROM PROGRAMMED
Z33	30-5603205	------	IC EPROM PROGRAMMED
Z34	30-5603206	------	IC EPROM PROGRAMMED
Z35	30-5603207	------	IC EPROM PROGRAMMED
Z36	30-5603208	------	IC EPROM PROGRAMMED

I/O BOARD, 30-7225801

REFERENCE	CHROMA PART NO.	MFG. NO.	DESCRIPTION
R1	30-1000909	------	POT ROTARY TRIMMER 10K ¼W 30%
R2	30-1003001	------	POT SLIDE LINEAR 10K ¼W 20%
C32	30-1103002	------	CAP ELECT 100UF 10V +50-10%
C1,2,3,4,6	30-1103005	------	CAP ELECT 10UF 35V 50-10%
C5	30-1103201	------	CAP ELECT 1UF 35V 20%
C20	30-1103202	------	CAP ELECT 22UF 35V 20%
CR23,24,25,26,27,31	30-1200201	4001	RECT 50V 1A
CR17-22,28,29,30	30-1200301	4148	DIODE SIGNAL
CR1,3,6,11,14	30-1201602	------	DIODE LIGHT EMIT 10MA GREEN
CR2,4,7,9,12,15	30-1201603	------	DIODE LIGHT EMIT 10MA RED
CR5,8,10,13,16	30-1201604	------	DIODE LIGHT EMIT 10MA YELLOW
Q2	30-1300501	2222	TSTR NPN GP
Q10	30-1301301	4392	TSTR N CHANNEL
Q3,4,5,6,7,8,9	30-1302901	3904	TSTR NPN GP
Q1	30-1305501	TIP29A	TSTR NPN PWR
Z2	30-1401101	1458	IC DUAL OP AMPL
Z48	30-1401702	74LS00	IC GATE 4X2I NAND
Z49,50	30-1402102	74LS10	IC GATE 3X3I NAND
Z55	30-1402201	7412	IC GATE 3X3I NAND OC
Z51	30-1402302	74LS20	IC GATE 2X4I NAND
Z21	30-1406401	4558	IC OP AMPL DUAL

I/O BOARD, 30-7225801 (contd.)

Z10,38	30-1406701	74LS74	IC DUAL D FF PRST CLEAR
Z25,53	30-1407601	081	IC OP AMPL FET
Z13	30-1408001	74LS145	IC DCD-DEC DECODER DRIVER
Z12,22,35,42	30-1409101	74LS175	IC QUAD D FLIP FLOP
Z20	30-1409702	7523J	IC 8 BIT CMOS DAC
Z11,44,45	30-1410501	74LS393	IC COUNTER DUAL 4 BIT
Z8	30-1411001	311	IC VOLTAGE COMP
Z18,19	30-1411601	4175	IC QUAD D FF
Z30	30-1411701	4174	IC HEX D FF
Z24	30-1412301	7541	IC 12 BIT CMOS DAC
Z31	30-1412401	8039	IC SINGLE COMP 8 BIT
Z3	30-1412501	0809	IC ADC 8 BIT 8 CHANNEL
Z5,6,23,26,36,46,47	30-1412801	74LS374	IC OCT D FF
Z15	30-1412802	74S374	IC OCTAL DUAL FLIP FLOP
Z32	30-1412901	74LS373	IC OCTAL DUAL FLIP FLOP TRAN
Z4,16,27,28,34,37	30-1413001	74LS244	IC OCT BUF 3 STATE
Z39,40,41	30-1413102	74LS138	IC 1 OF 8 DECODER
Z29	30-1413201	74LS174	IC HEX DUAL FLIP FLOP
Z43	30-1413401	74LS153	IC DUAL 4 CHANNEL
Z9	30-1413701	MCT66	IC DUAL OPTO COUPLE
Z14	30-1414101	-----	IC RES NETWORK 16 PIN 220 OHM ¼W 2%
Z52	30-1414102	-----	IC RES NETWORK 16 PIN 100 OHM ¼W 2%
Z17	30-1414103	-----	IC RES NETWORK 16 PIN 10K ¼W 2%
Z54	30-1414104	-----	IC RES NETWORK 16 PIN 1K ¼W 2%
Z1	30-1414701	324	IC OP AMPL
I1	30-1800901	-----	DISPLAY LED 7 SEG 2 DIGIT RED
I2	30-1801001	-----	DISPLAY LED 7 SEG 8 DIGIT RED
J22	30-2101301	-----	SOCKET DUAL IN LINE 14 PIN
J20,24	30-2101302	-----	SOCKET DUAL IN LINE 16 PIN
For Z10,38	30-2102702	-----	SOCKET DUAL IN LINE 14 PIN LP
For Z20	30-2102703	-----	SOCKET DUAL IN LINE 16 PIN LP
For Z33	30-2102705	-----	SOCKET DUAL IN LINE 24 PIN LP
For Z31	30-2102706	-----	SOCKET DUAL IN LINE 40 PIN LP
For Z24	30-2102707	-----	SOCKET DUAL IN LINE 18 PIN LP
For Z5,6,15	30-2102708	-----	SOCKET DUAL IN LINE 20 PIN LP
For Z3	30-2102709	-----	SOCKET DUAL IN LINE 28 PIN LP
J12	30-2102902	-----	CONN PLUG WAFER 3 PIN
J13	30-2104402	-----	CONN WAFER PC BD 6 PIN
J18	30-2104404	-----	CONN WAFER PC BD 10 PIN
J11	30-2104406	-----	CONN WAFER PC BD 4 PIN
J14,15,16	30-2106801	-----	CONN FLAT COND 10 PIN
J9,10	30-2107401	-----	CONN RECPT SIP 15 POS
J17	30-2107501	-----	CONN RECPT MALE 26 PIN RT ANGLE
	30-2107601	-----	LATCH EJECTOR
J1,2	30-2108001	-----	CONN WAFER PC BD 6 PIN
Z33	30-5603301	-----	IC EPROM PROGRAMMED KEYBOARD SCAN

CHANNEL MOTHER BOARD, 30-7225401

REFERENCE	CHROMA PART NO.	MFG. NO.	DESCRIPTION
C13,14	30-1103002	-----	CAP ELECT 100UF 10V 20%
C4	30-1103004	-----	CAP ELECT 220UF 6.3V +50-10
C1	30-1103005	-----	CAP ELECT 10UF 35V 50-15%
C2,3	30-1103007	-----	CAP ELECT 1000UF 16V +50-10
CR2	30-1200101	1N34A	DIODE GE
CR1	30-1200301	4148	DIODE SIGNAL
Q1,2	30-1302901	3904	TSTR NPN GP
Z4,6	30-1404402	4013B	IC DUAL D FF SET/RESET
Z16,17	30-1404501	4016B	IC QUAD BILAT SWITCH
Z7	30-1405101	4071B	IC GATE 4X2I OR
Z18,19	30-1406401	4558	IC OP AMPL DUAL

Z20	30-1411001	311	IC VOLTAGE COMPARATOR
Z1,2,5	30-1411601	4175	IC QUAD DUAL FLIP FLOP
Z3	30-1411701	4174	IC HEX DUAL FLIP FLOP
Z14,15	30-1414201	5837/2688	IC NOISE GEN
Z8,9,10,11,12,13	30-1414301	4556	IC 1 OF 4 DECODER DUAL
J5-0,1,2,3,4,5,6,7	30-2104403	------	CONN WAFER PC BD 8 PIN
J7-0,1,2,3,4,5,6,7			
J8-0,1,2,3,4,5,6,7			
J6-0,1,2,3,4,5,6,7	30-2108601	------	CONN WAFER PC BD 8 PIN
P24	30-2200807	------	CABLE RIBBON 26 AWG 16 PIN 24"

DUAL CHANNEL BOARD, 30-7225601

REFERENCE	CHROMA PART NO.	MFG. NO.	DESCRIPTION
R3,4,5,6	30-1000105	------	RES WW TC 1.87K 1W 3%
R1,2	30-1001607	------	POT ROTARY TRIMMER 10K 1/5W 30%
C1,2,3,4	30-1102301	------	CAP PLASTIC FILM .001UF 100V 10%
C15	30-1103005	------	CAP ELECT 10UF 35 V 50-10%
C13,14,16,17,18	30-1103201	------	CAP ELECT 1UF 35V 20%
C32,33,34,35,36,37,38,39	30-1103901	------	CAP POLY FILM .0068UF 50V 10%
C24,25,26,27,28,29,30,31	30-1103902	------	CAP POLY FILM .033UF 50V 10%
CR1,2	30-1200301	4148	DIODE GE
Q1,4,5,8,9	30-1302901	3904	TSTR NPN GP
Q2,3,6,7	30-1303001	3906	TSTR PNP GP
Z1	30-1400501	3086	IC TSTR ARRAY
Z7	30-1400601	4011U	IC GATE 4X2I NAND
Z19,20	30-1404901	4051B	IC SINGLE 8-CHAN MULTIPLEXER
Z12	30-1406201	4053B	IC TRIPLE 2-CHAN MULTIPLEXER
Z4,10,29	30-1406401	4558	IC OP AMPL DUAL
Z5,14,21,22,23,24	30-1409001	082/353	IC OP AMPL DUAL FET
Z8,9,11,15,17,18	30-1409501	4052B	IC DUAL 4-CHAN MULTIPLEXER
Z26,27,28	30-1411701	4174	IC HEX DUAL FLIP FLOP
Z6	30-1413601	393	IC DUAL COMPARATOR OC
Z2,3	30-1413901	4151	IC VCF CHARGE PUMP
Z25	30-1414301	4556	IC 1 OF 4 DECODER DUAL
Z16	30-1414401	3360	IC DUAL VCA
Z13	30-1414501	3350	IC DUAL VCF

LEFT STACK SWITCH ASSEMBLY, 30-7543601

REFERENCE	CHROMA PART NO.	MFG. NO.	DESCRIPTION
Z1	30-1408001	74LS145	IC BCD-DEC DECODER DRIVER
Z2,3,4,5	30-1414103	------	IC RES NETWORK 16 PIN 10K ¼W 2%
For P21	30-2107701	------	CONN HOUSING FLAT FLEX 15 PIN
P21	30-2204701	------	CABLE FLAT FLEX 15 COND 2.5"
	30-5710701	------	SWITCH LEAF LOW BOUNCE

RIGHT STACK SWITCH ASSEMBLY, 30-7543701

REFERENCE	CHROMA PART NO.	MFG. NO.	DESCRIPTION
Z7,8	30-1405401	339	IC QUAD COMP
Z1	30-1408001	74LS145	IC BDC-DEC DECODER DRIVER
Z6	30-1414102	------	IC RES NETWORK 16 PIN 100 OHM ¼W 2%
Z2,3,4,5,9	30-1414103	------	IC RES NETWORK 16 PIN 10K ¼W 2%
J21	30-2107401	------	CONN RECPT SIP 15 POS
P20	30-2200805	------	CABLE RIBBON 26 AWG 16 PIN 9"
	30-5710701	------	SWITCH LEAF LOW BOUNCE

EQ BOARD, 30-7225501

REFERENCE	CHROMA PART NO.	MFG. NO.	DESCRIPTION
R1,5	30-1002901	-----	POT SLIDE LINEAR 10K 1/5W 20%
R2,3,4	30-1002902	-----	POT SLIDE LINEAR 100K 1/5W 20%
C20,21	30-1102901	-----	CAP ELECT NP 10UF 16V +50-10%
C18	30-1103001	-----	CAP ELECT 4.7UF 35V +100-10%
C1,2	30-1103005	-----	CAP ELECT 10UF 35V +50-10%
CR1,2,3,4,5	30-1200301	4148	DIODE SIGNAL
Q4,6	30-1300401	2907	TSTR PNP GP
Q3,5	30-1300501	2222	TSTR NPN GP
Q2	30-1302901	3904	TSTR NPN GP
Q1	30-1304901	5485	TSTR N CHAN FET
Z3,4,5,6	30-1406401	4558	IC OP AMPL DUAL
Z1,2	30-1414401	3360	IC VCA DUAL
J25	30-2104402	-----	CONN WAFER PC BD 6 PIN
J19	30-2104408	-----	CONN WAFER PC BD 14 PIN
J4	30-2108002	-----	CONN WAFER PC BD 3 PIN

POWER SUPPLY ASSY, 30-7543901

REFERENCE	CHROMA PART NO.	MFG. NO.	DESCRIPTION
R12	30-1000112	-----	RES WW .120 OHMS 1W 5%
R18,25,30	30-1000113	-----	RES WW 1K 1W 10%
R22	30-1000909	-----	POT ROTARY TRIMMER 10K ¼W 30%
R46	30-1001601	-----	POT ROTARY TRIMMER 100K 1/5W 30%
R1,2	30-1002801	-----	VARISTOR METAL OXIDE 150VAC
C7,11	30-1101301	-----	CAP ELECT 1000UF 50V 75-10%
C6,9,15,16	30-1103005	-----	CAP ELECT 10UF 35V 50-10%
C10,12	30-1103401	-----	CAP ELECT 3.3UF 35V +100-10%
CR13	30-1200101	34A	DIODE GE
CR11,12,15,16	30-1200301	4148	DIODE SIGNAL
CR4	30-1200505	5257	DIODE ZENER 33V 5%
CR14	30-1200506	5228B	DIODE ZENER 3.9V 5%
CR1,2	30-1201701	MR750	DIODE RECT 50V 6A
CR3,5	30-1201901	4742	DIODE ZENER 12V 5%
CR6,7,8,9,10	30-1202101	4002	DIODE 100V 1A
Q3,5,8,10,13	30-1302901	3904	TSTR NPN GP
Q11,12	30-1303001	3906	TSTR PNP GP
Z3	30-1414801	589KH	IC VOLTAGE REFERENCE
Z1,2	30-1415101	358	IC DUAL OP AMPL
	30-1700801	-----	FUSE CLIP
J1,2,3	30-2108001	-----	CONN RECPT PC BD 6 PIN
J4	30-2108002	-----	CONN RECPT PC BD 3 PIN
C3	30-1104001	-----	CAP ELECT 47000UF 7.5V 75-10%
Q7,9	30-1305301	TIP110	TSTR NPN DARL
Q6	30-1305501	TIP29A	TSTR NPN PWR
Q2,4	30-1306401	IRF531	TSTR MOS FET POWER
Q1	30-1306501	6258	TSTR NPN PWR
	30-1901501	-----	SWITCH SLIDE DPDT
S1	30-1905101	-----	SWITCH SLIDE DPDT 115V/230V UL
	30-2103101	-----	CONN RECPT 3 PIN
	30-2108201	-----	CONN RECPT 5 PIN
T1	30-5710601	-----	TRANSFORMER POWER
	30-7226001	-----	PC BD ASSY OVERVOLTAGE PROTECTOR

SECTION 8. MNEMONICS

RD = READ
WR = WRITE

RD	ADCI	A/D converter data input
	MSCI	Miscellaneous input
	EXTI	External computer interface input
	TIME	Timer reading (requires both strobes)
	TIME + 1	Timer reading (requires both strobes)
	SWB	Switch bank (panel)
	NOTE	Note number (keyboard)
	VEL	Velocity value (keyboard)
	EOC	End of conversion
WR	ADCO	A/D converter channel select (starts conversion)
	MSCO	Miscellaneous output
	EXTO	External computer interface output
	TMOD	Timer mode
	SEGS	Display segments
	SDS	Switch bank and display digit select
	LEDS	LEDS
	LEDS + 1	LEDS
WR	SYND	Synthesizer data latch (Mother Board)
	SYNA	Synthesizer address latch (Mother Board)
	RDAC	Reference 8 Bit D/A converter
	SHA	Sample and hold address
	MDAC	Main 12 Bit D/A converter (requires both strobes)
	MDAC + 1	Main 12 Bit D/A converter (requires both strobes)
	PRSS	Pressure sensor select
	TAP	Tapper
XI	FULL	External computer interface input buffer full
XI	ACK	External computer interface input ackowledge
XI	INT	External computer interface input interrupt
XO	FULL	External computer interface output buffer full
XO	ACK	External computer interface output acknowledge
XO	INT	External computer interface output interrupt
	TRDY	Timer ready
	KINT	Keyboard interrupt